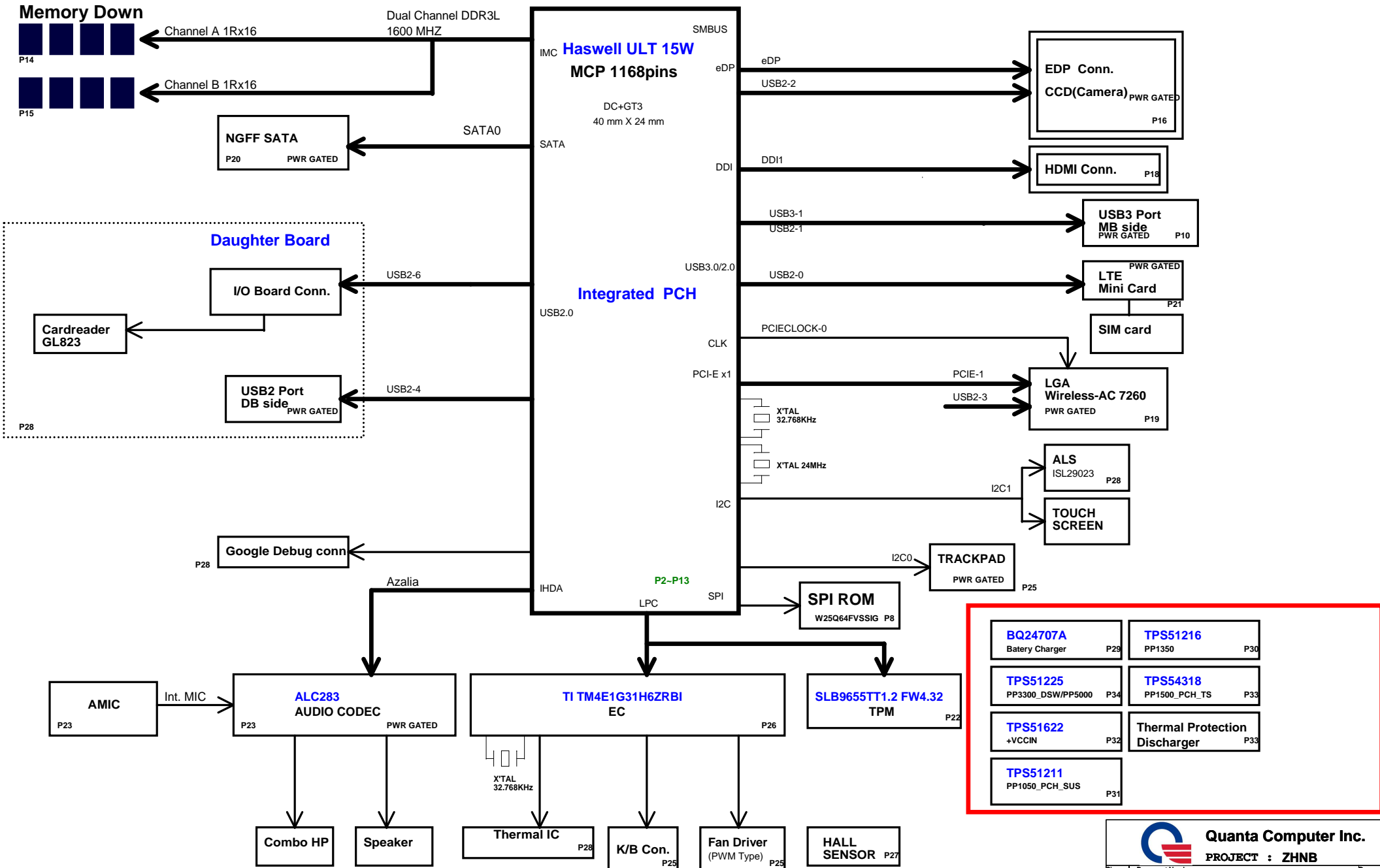
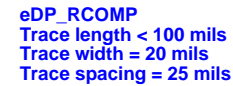


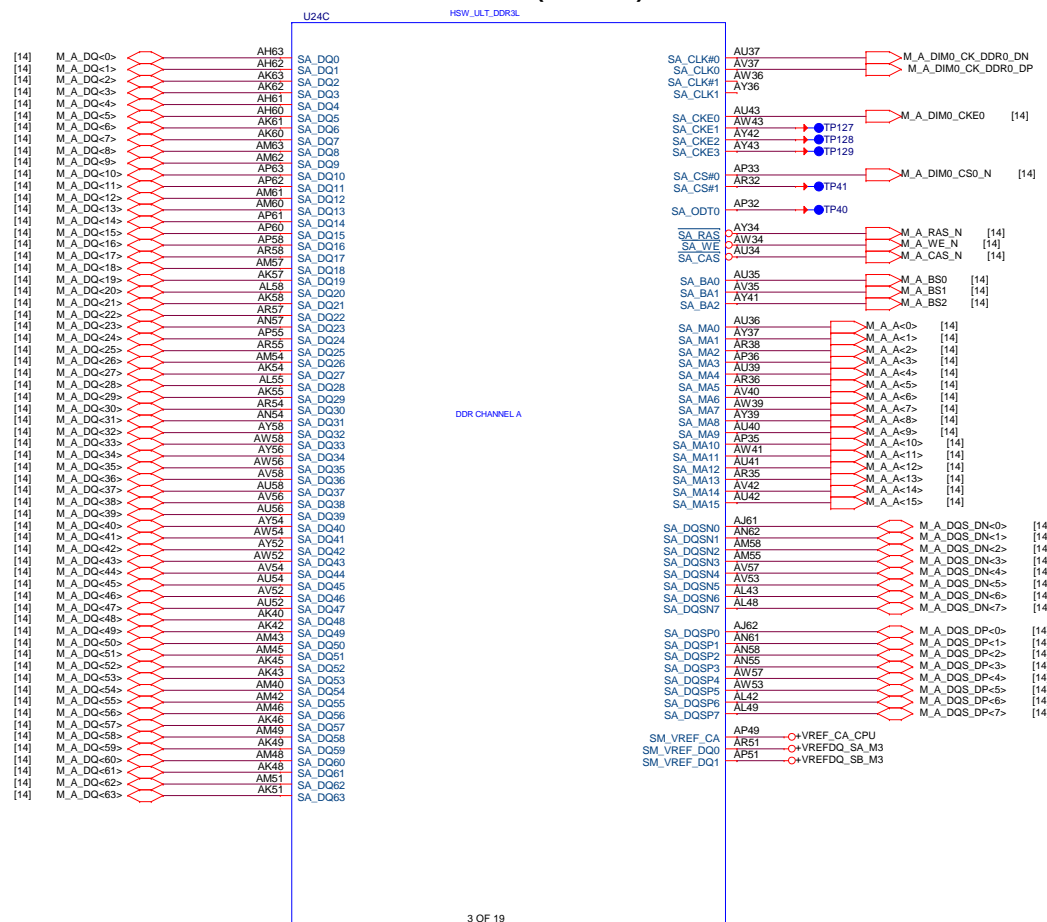
Benetton_EDU(ZHNB) SHB ULT SYSTEM BLOCK DIAGRAM





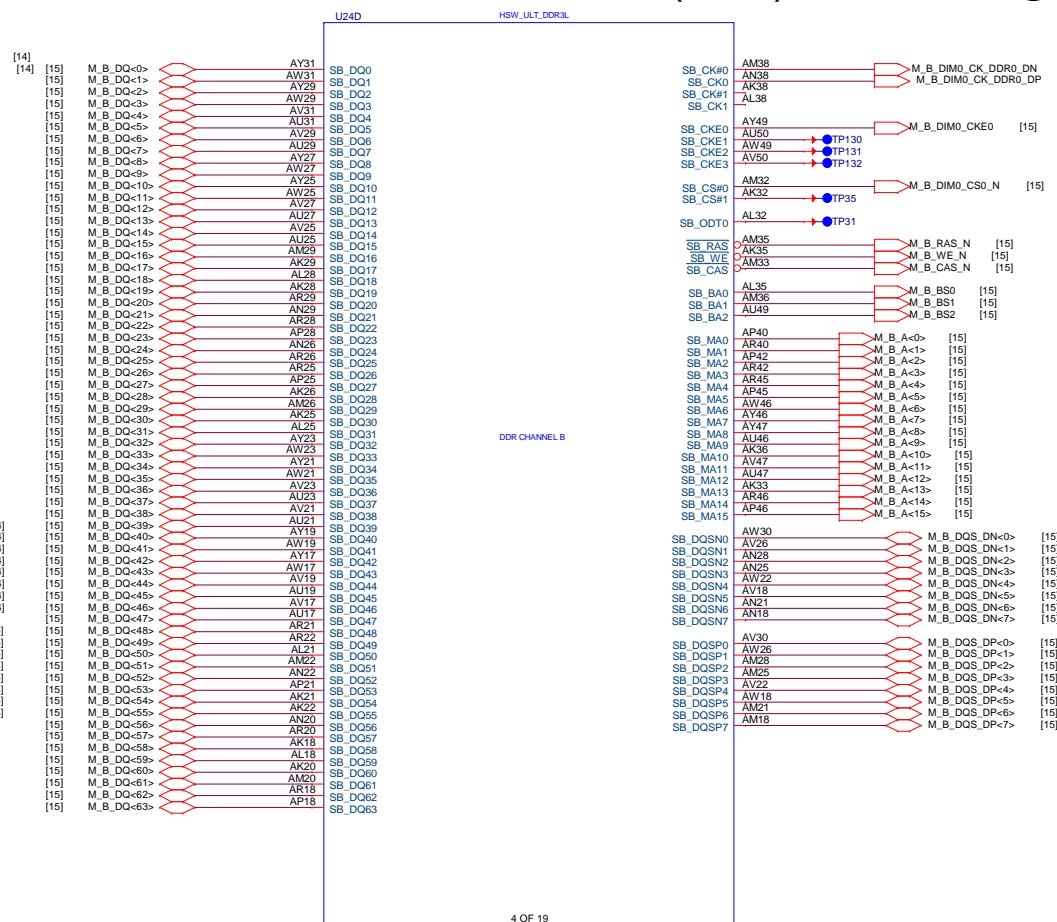
Date: Thursday, December 04, 2014 Sheet 2 of 39

Haswell ULT (DDR3L)



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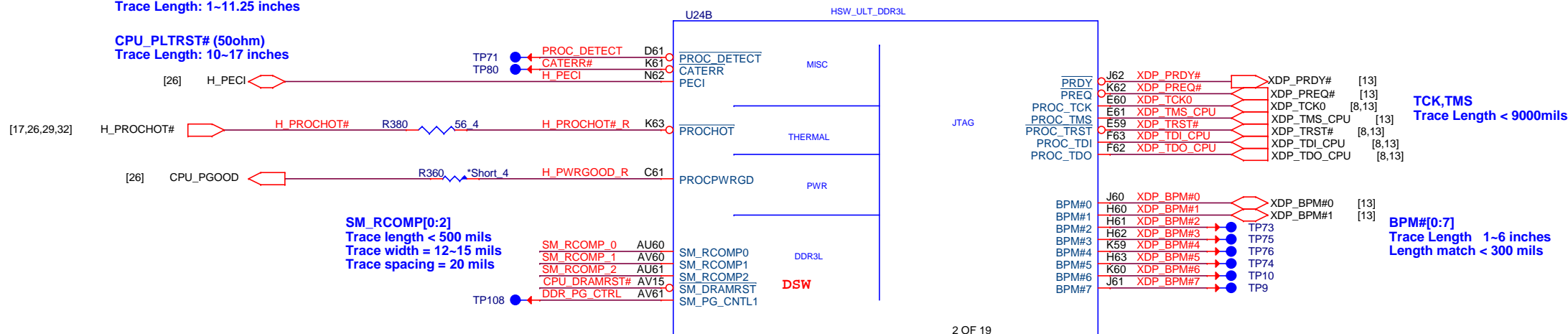
Haswell Processor (DDR3L)



4 OF 19

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



The schematic shows the XDP_TDO_CPU pin connected to a pull-up resistor R29 to the +1.05V_VCCST supply. The pin is also connected to the XDP_TCK0 and XDP_TRST# pins, which are connected to a pull-up resistor R433 and R462 to the 51.4V supply.



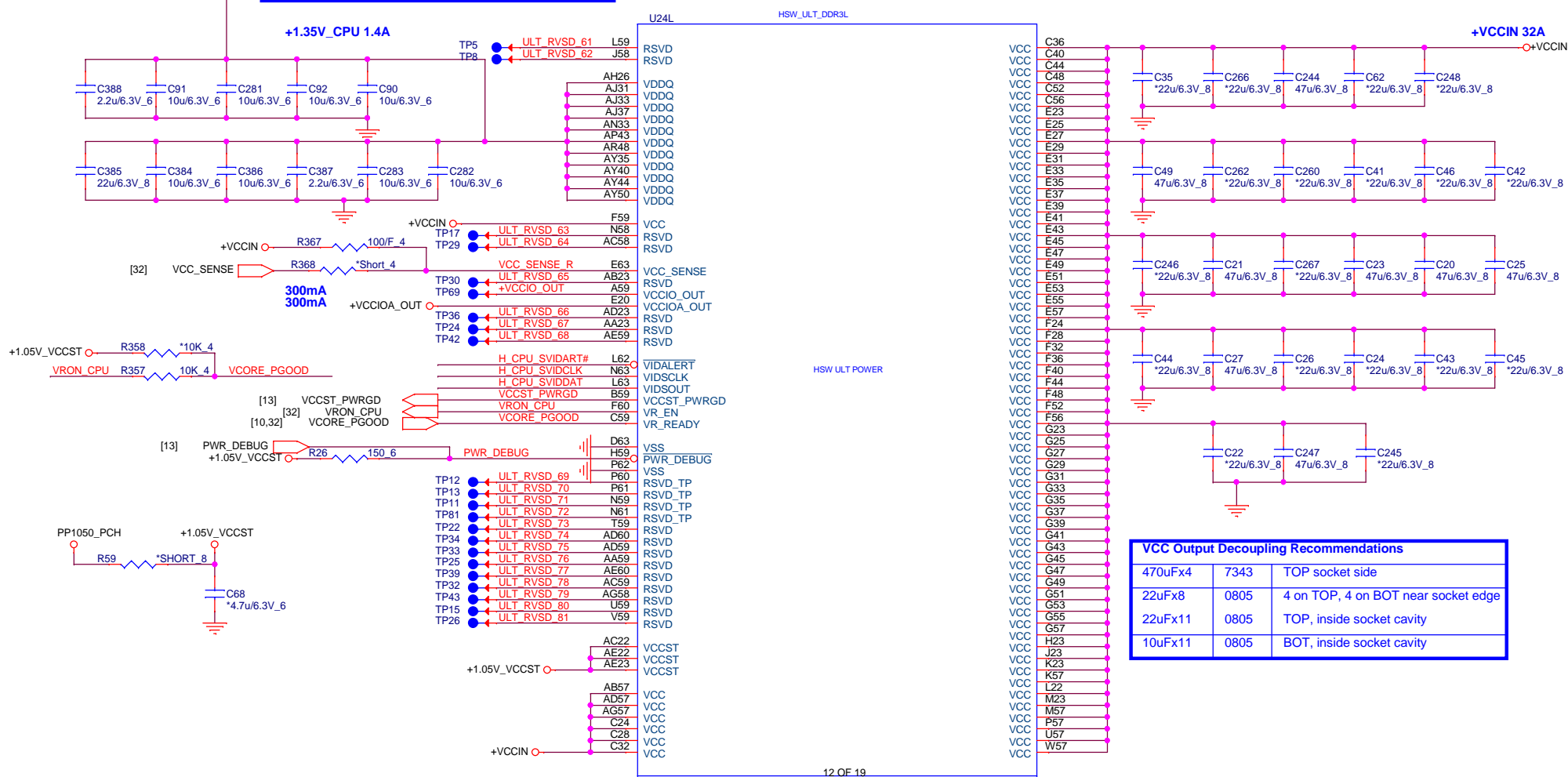
PROJECT : ZHNB

Size	Document Number	Rev
	Haswell 3/5 (SideBand)	A
Date:	Thursday, December 04, 2014	Sheet 4 of 39

Haswell ULT (POWER)

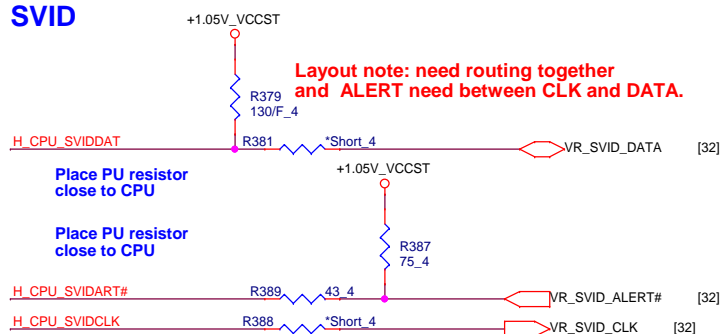
VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity

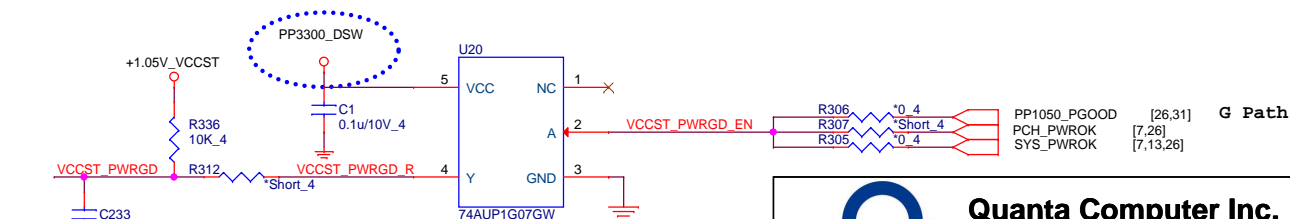


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SVID



VCCST PWRGD

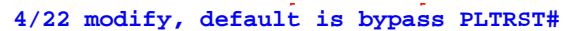




	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	



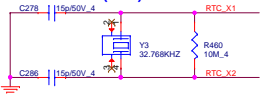
07



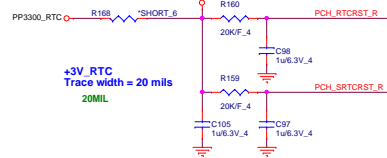
PROJECT : ZHNB

Size	Document Number PCH 1/6 (PM)	Rev A
Date:	Thursday, December 04, 2014	Sheet 7 of 39

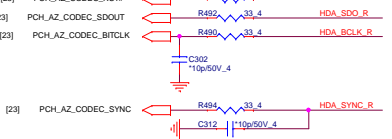
RTC Clock 32.768KHz (RTC)



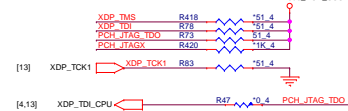
RTC Circuitry (RTC)

+3V_RTC
Trace width = 30 mils+3V_RTC
Trace width = 20 mils
20MIL

HDA



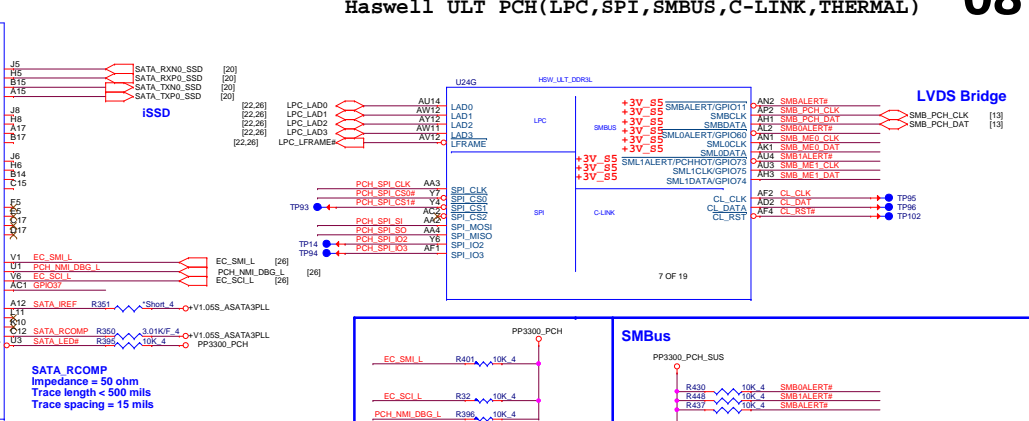
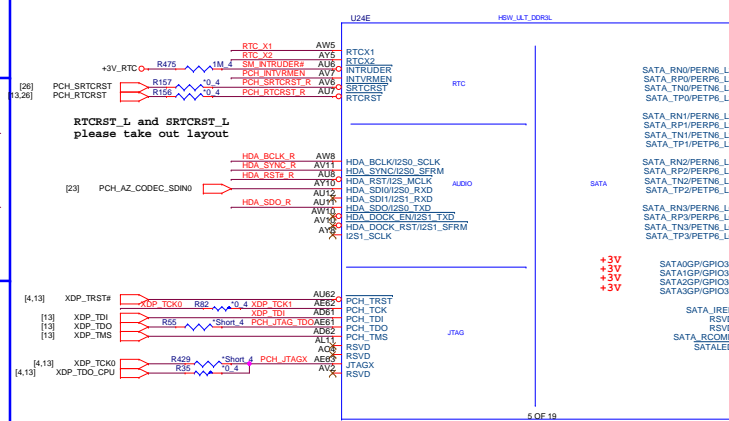
PCH JTAG

JTAG TCK,JTAG TMS
Trace Length < 9000mils

ULT Strapping Table

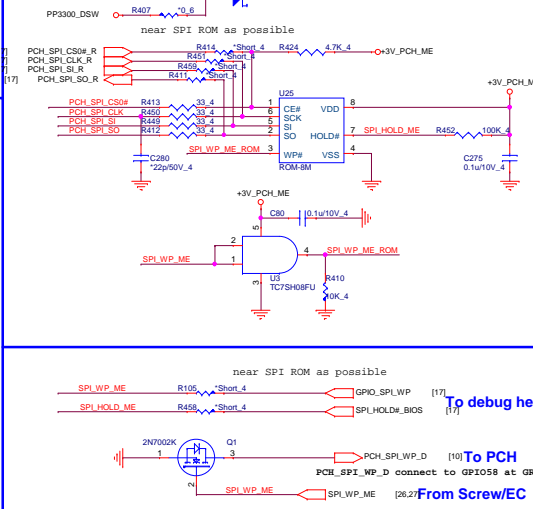
Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (IPD 20K) 1 = Disable No-Reboot mode	PP3300_PCH R400 *1K_4 SPKR [10,23]
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (IPD 20K) 1 = can't program ME	HDA_SDO_R R493 *0.4 PCH HDA_SDO [26]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	+3V_RTC R484 *330K_4 PCH INTRVEMEN R485 *330K_4
GPIO66	Top-Block Swap override		0 = Default disable (IPD 30K) 1 = Enable TBS function	PP3300_PCH R330 *1K_4 GPIO66 R340 *1K_4
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (IPD 20K) 1 = LPC	PP3300_PCH R1 GPIO86 R7 *1K_4
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(IPD 20K) 1 = Default enable with confidentiality	PP3300_PCH_SUS GPIO15 R50 *8.2K_4 GPIO15 R58 *1K_4
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 = disable	[6,13] CFG4 R64 *1K_4
DSWVREN	Deep Sx well on the VR enable		1=Should be always pull-up	+3V_RTC R476 *330K_4 DSWVREN R472 *330K_4

Haswell ULT PCH (RTC/HDA/SATA/SPI)



PCH dual I/O SPI ROM

W25Q64FVS8IG(801C) / AKE3EFP0N06----->8MB



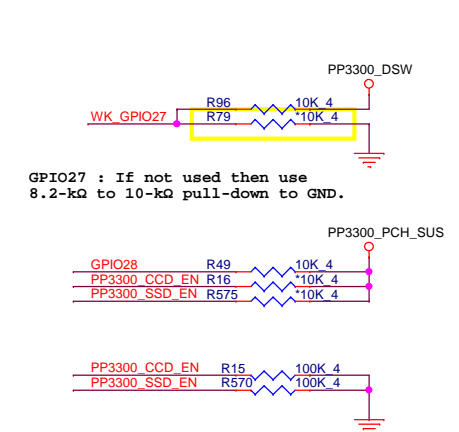
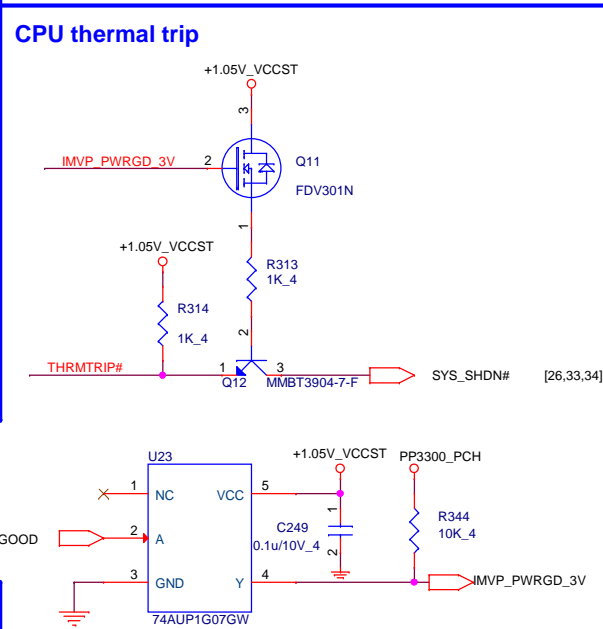
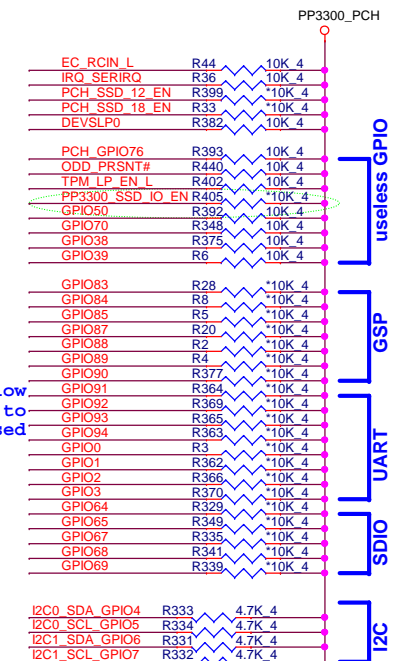
09



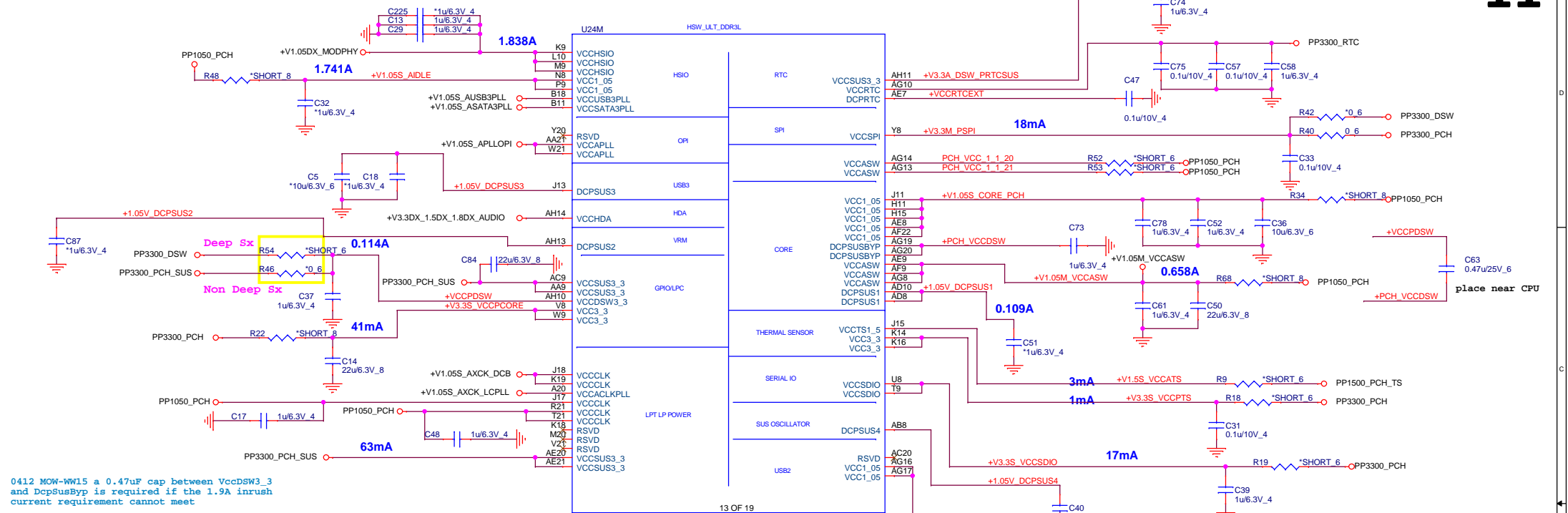
09



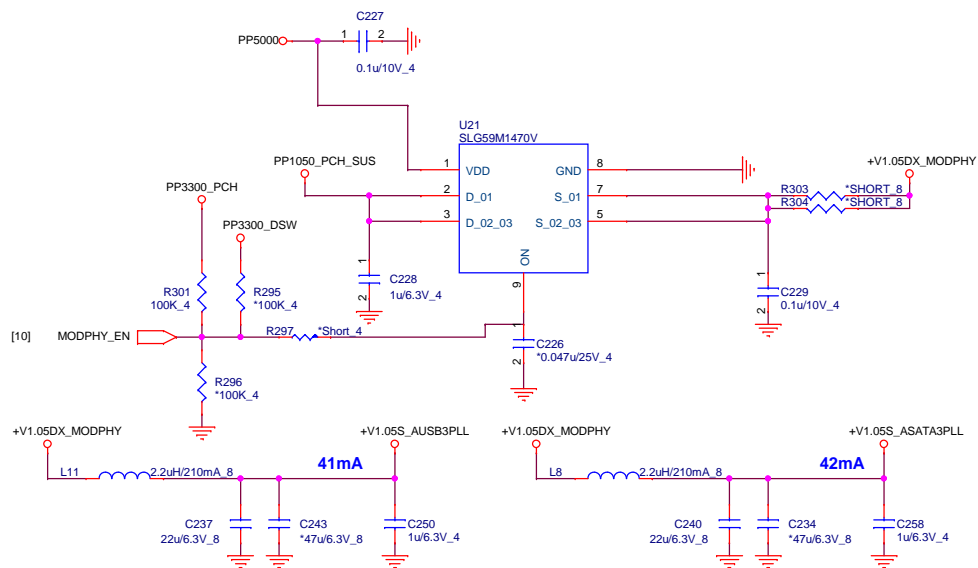
10



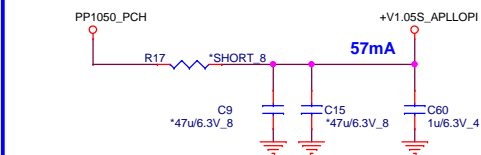
Haswell ULT PCH (Power)



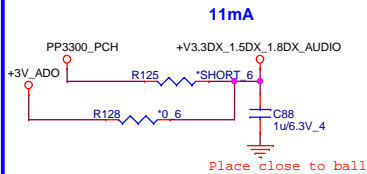
PCH VCCHSIO Power



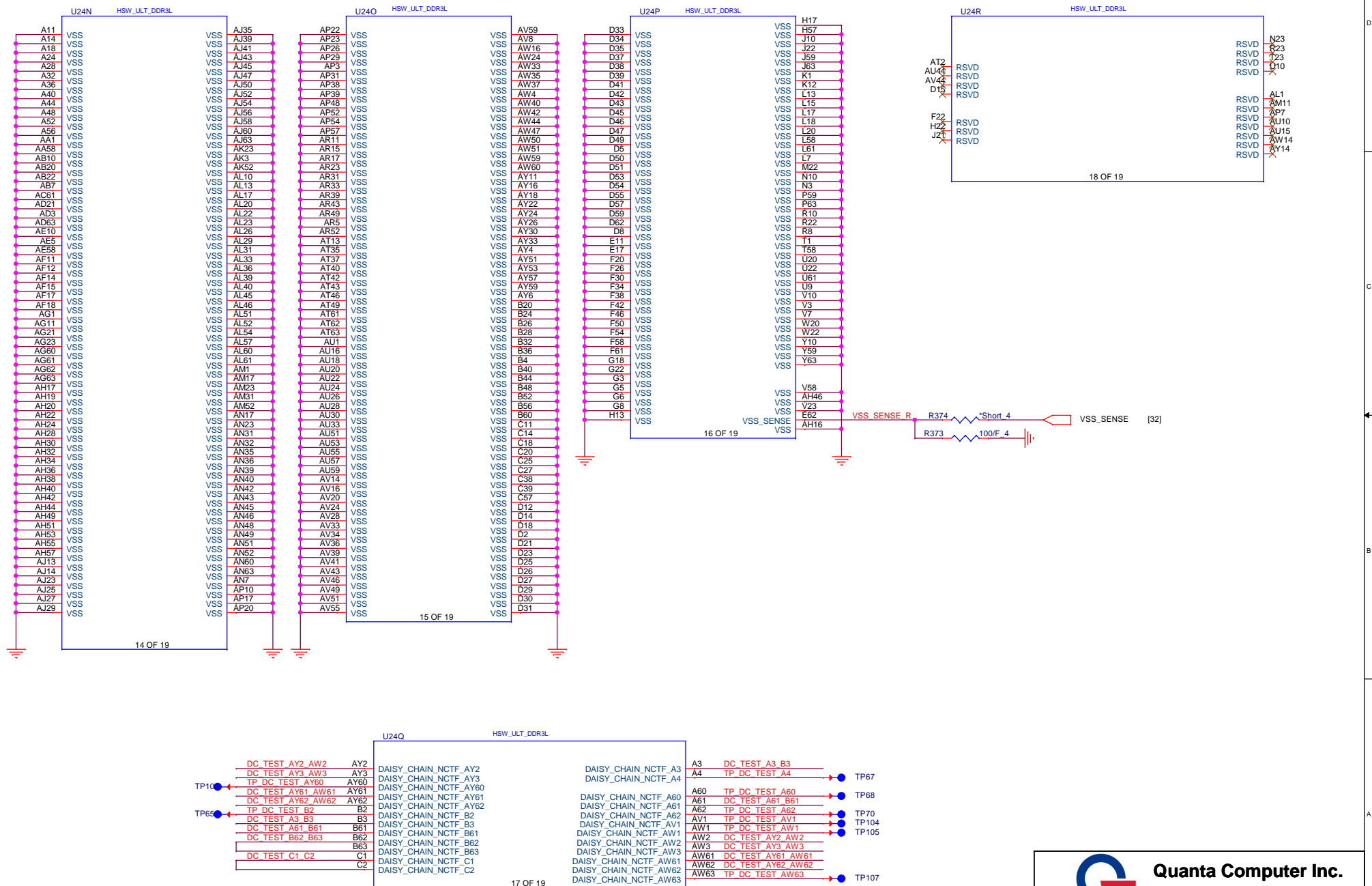
VCCAPLL power

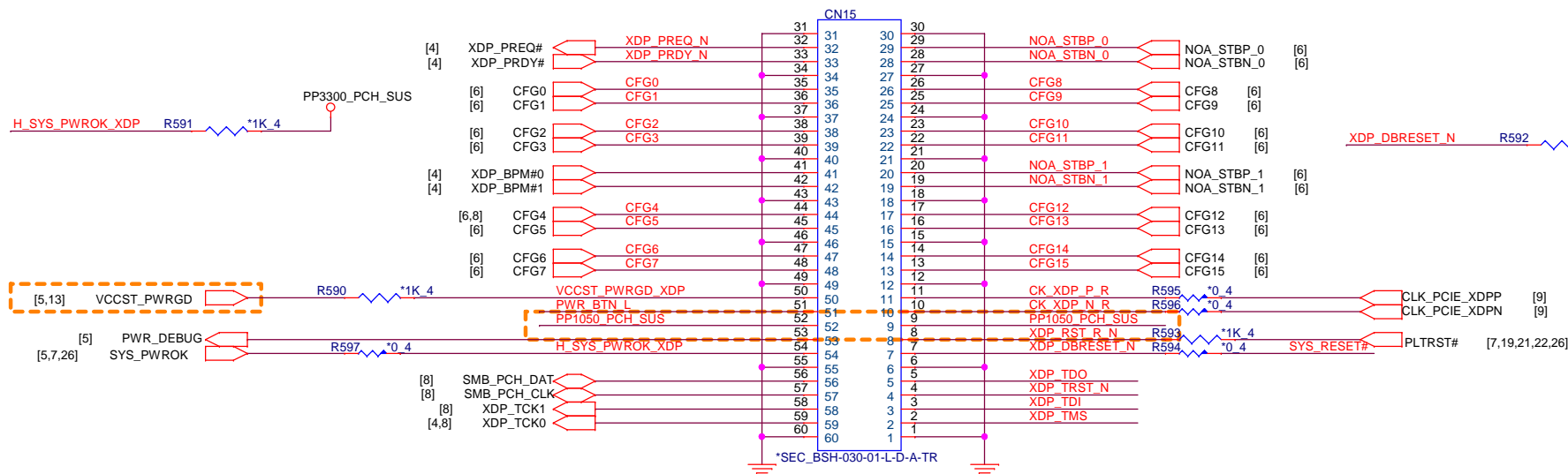


PCH HDA Power

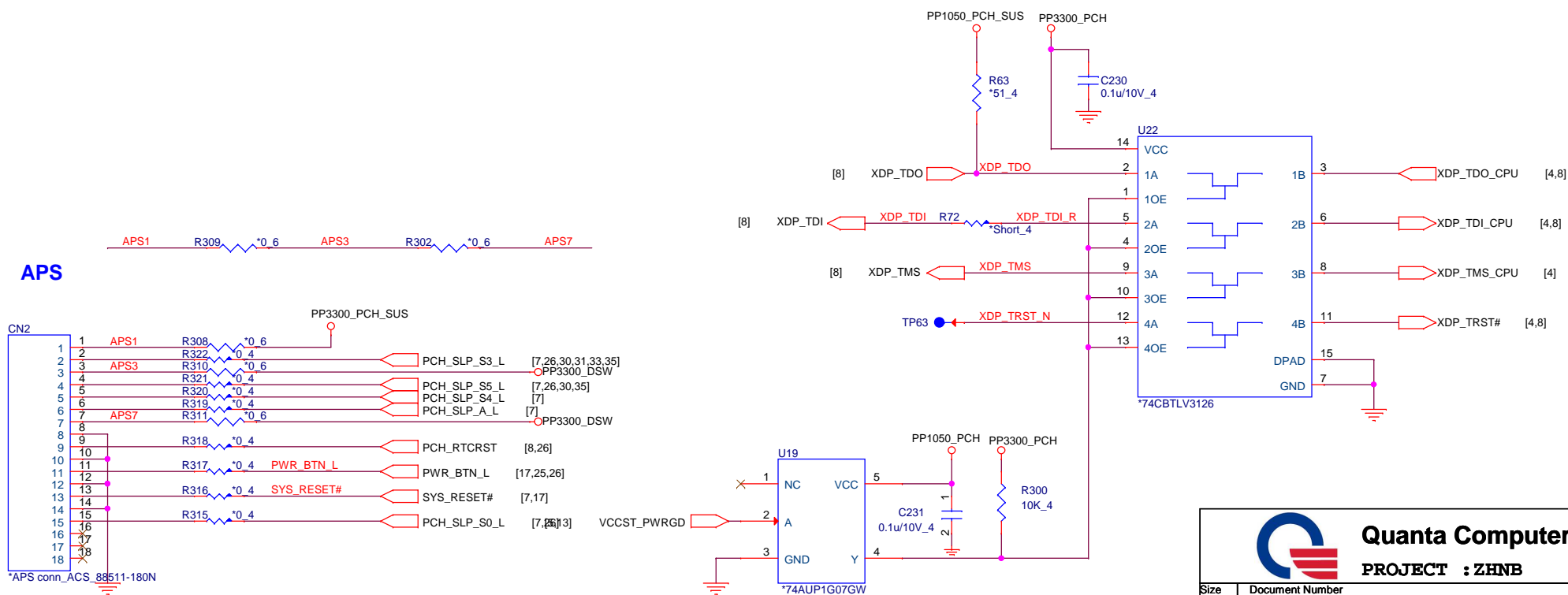


Haswell ULT (GND)



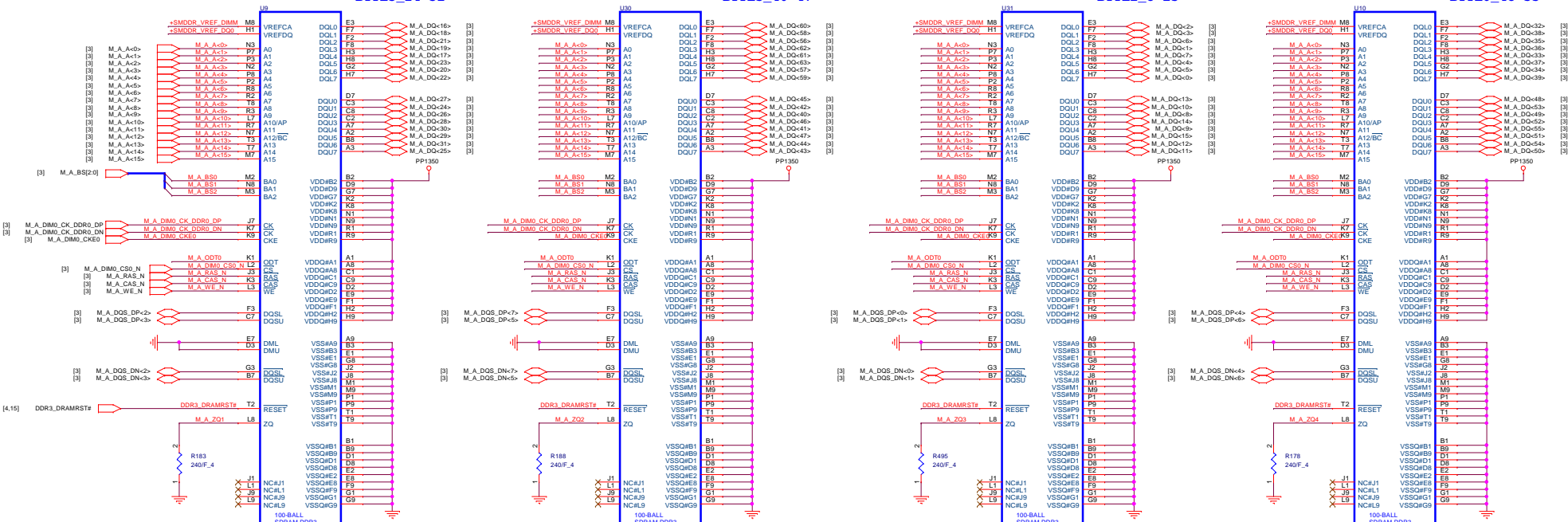


20141021 Intel require modify ITP CN15 P9/P51 add PP1050_PCH_SUS, P50 PP1050_PGOOD change to VCCST_PWRGD.



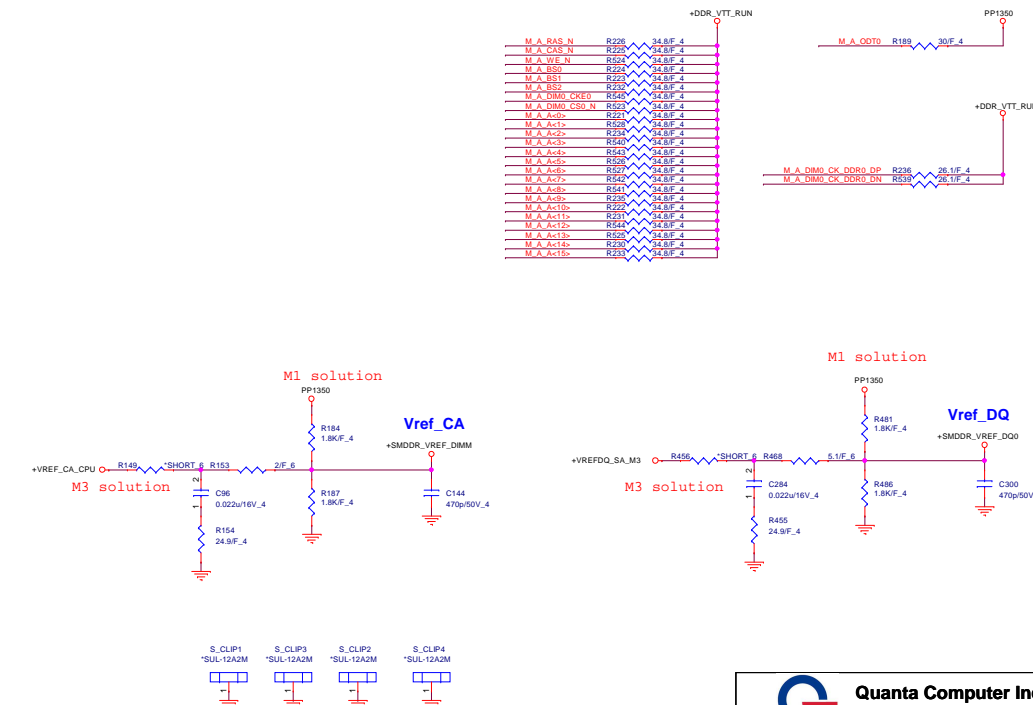
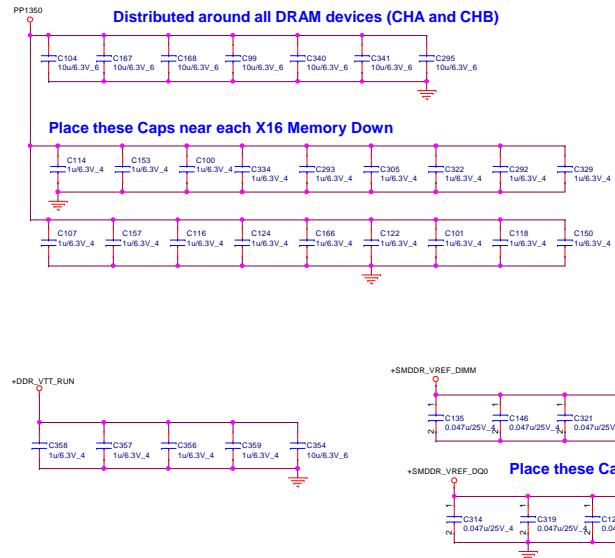
BYTE4_32-3

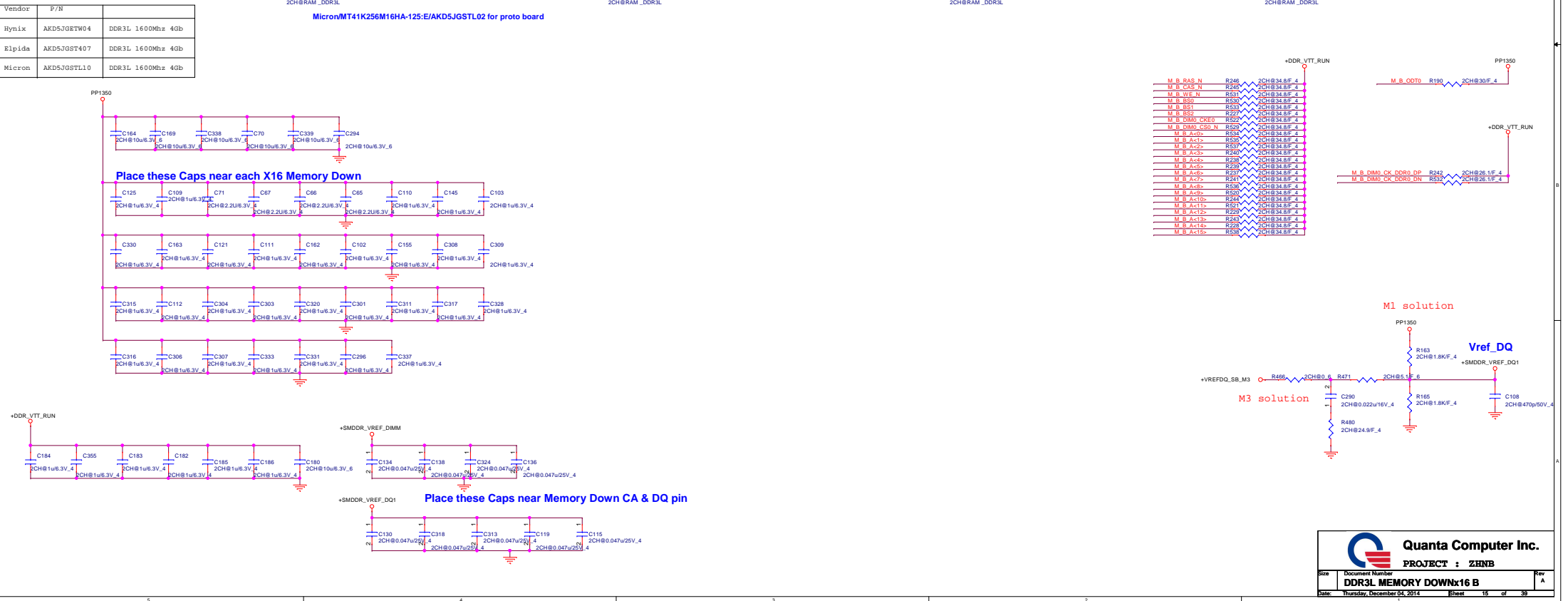
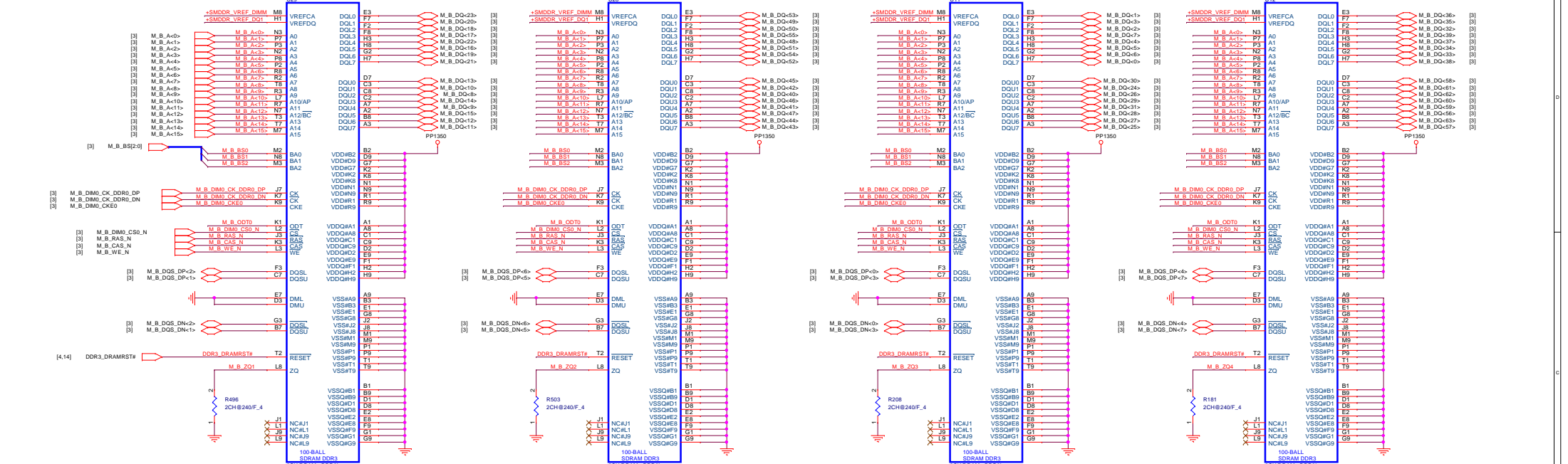
BYTE6 48-5



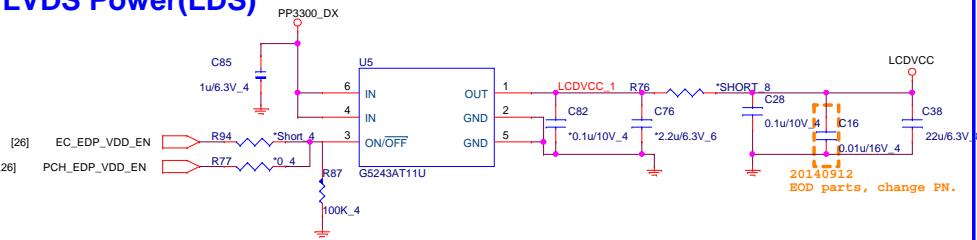
Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

Micron/MT41K256M16HA-125:E/AKD5JGSTL02 for proto board

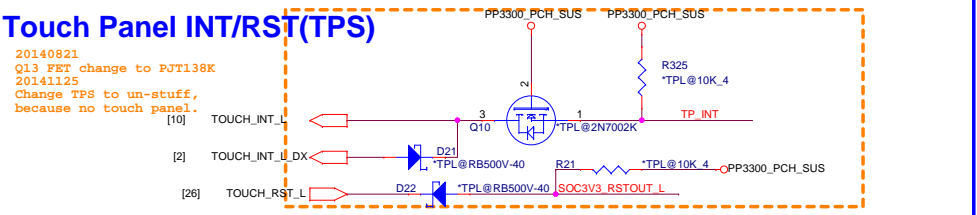




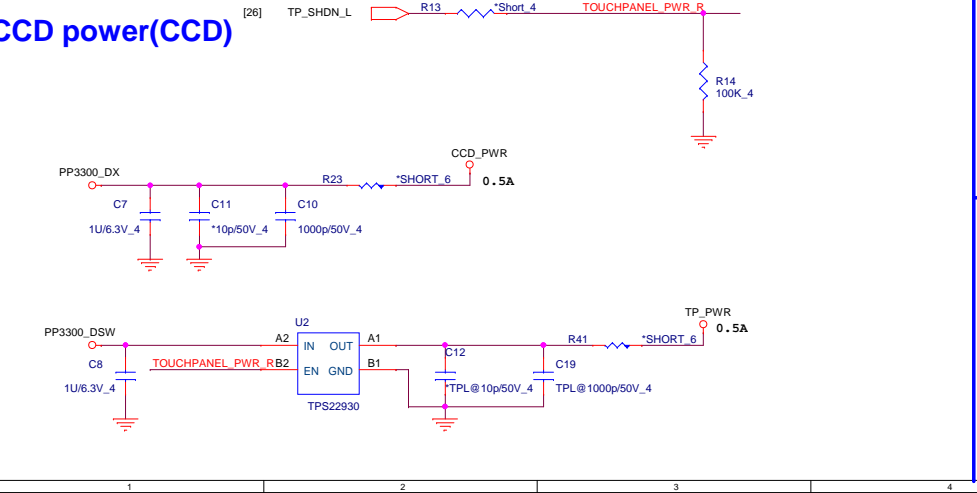
LVDS Power(LDS)



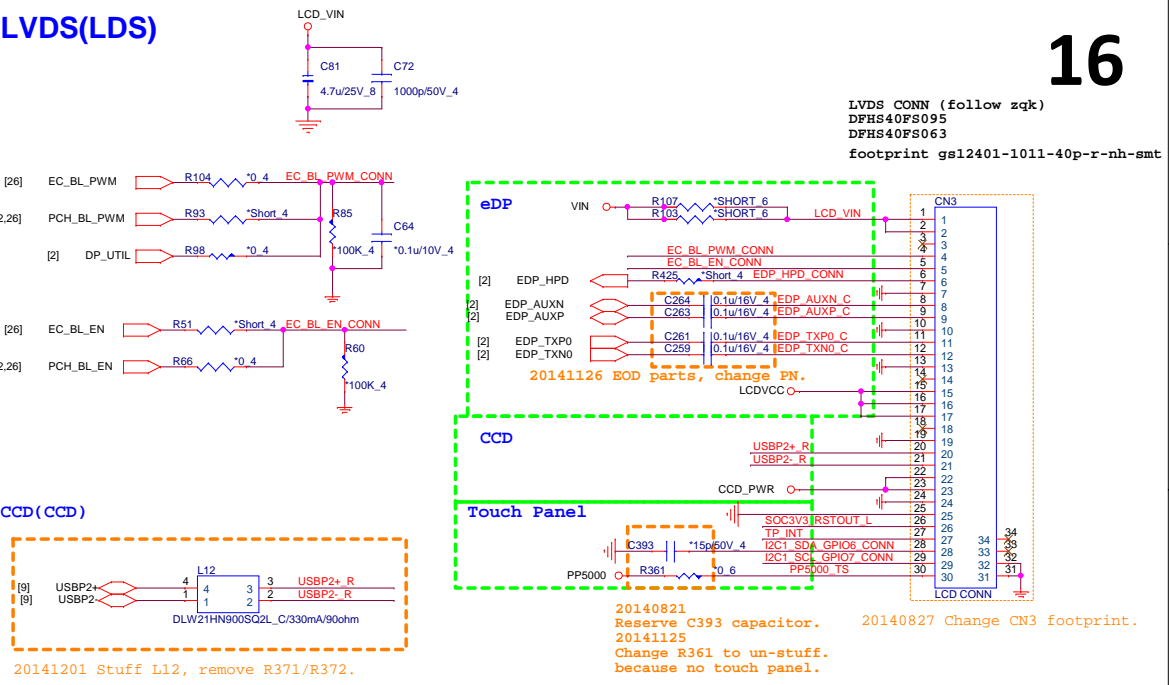
Touch Panel INT/RST(TPS)



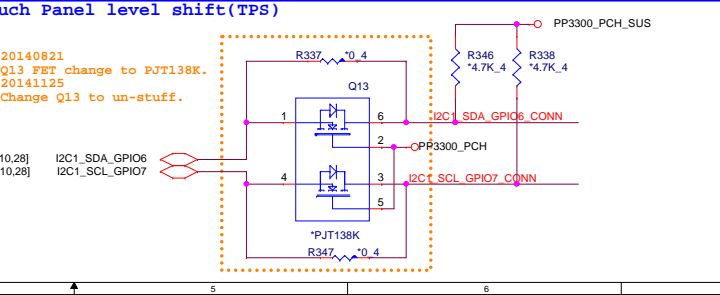
CCD power(CCD)




LVDS(LDS)



Touch Panel level shift(TPS)





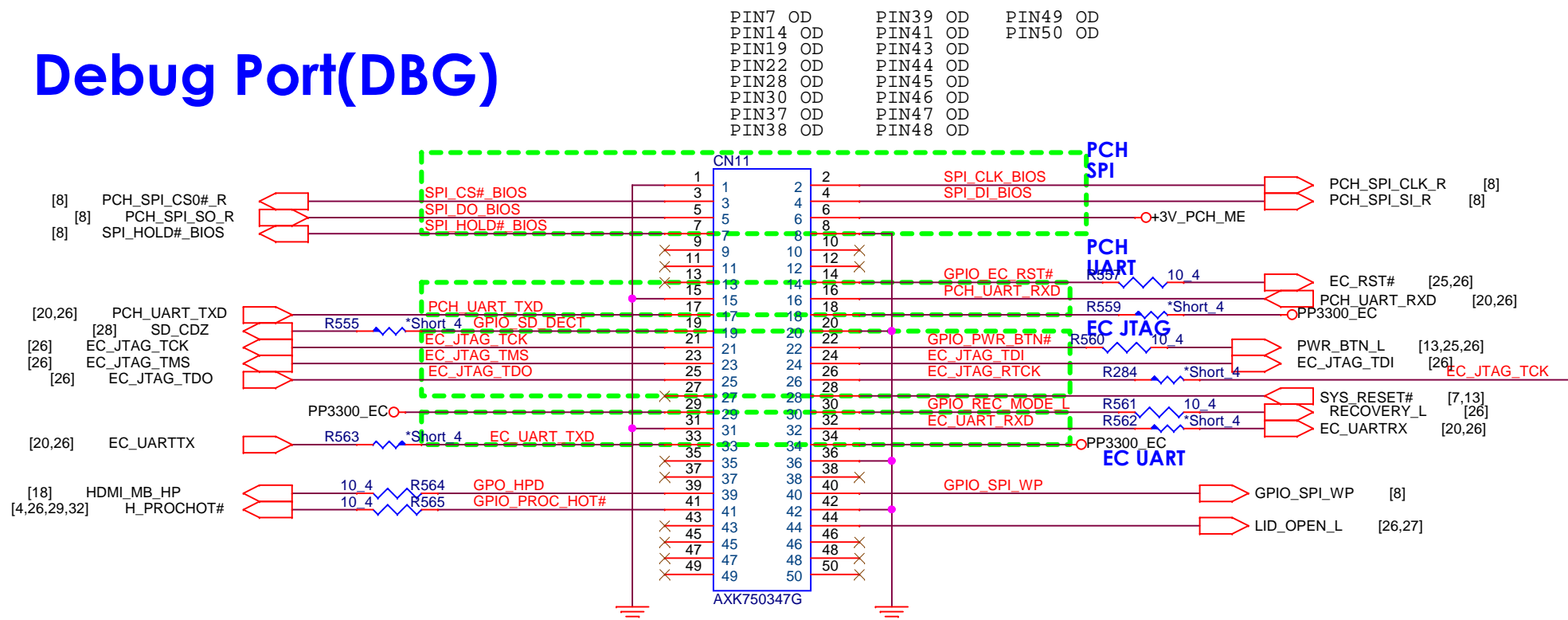
Quanta Computer Inc.

PROJECT : ZHNB

LVDS/CCD/DMIC/TS

Size	Document Number	Rev
Date	Thursday, December 04, 2014	Sheet 16 of 39

Debug Port(DBG)

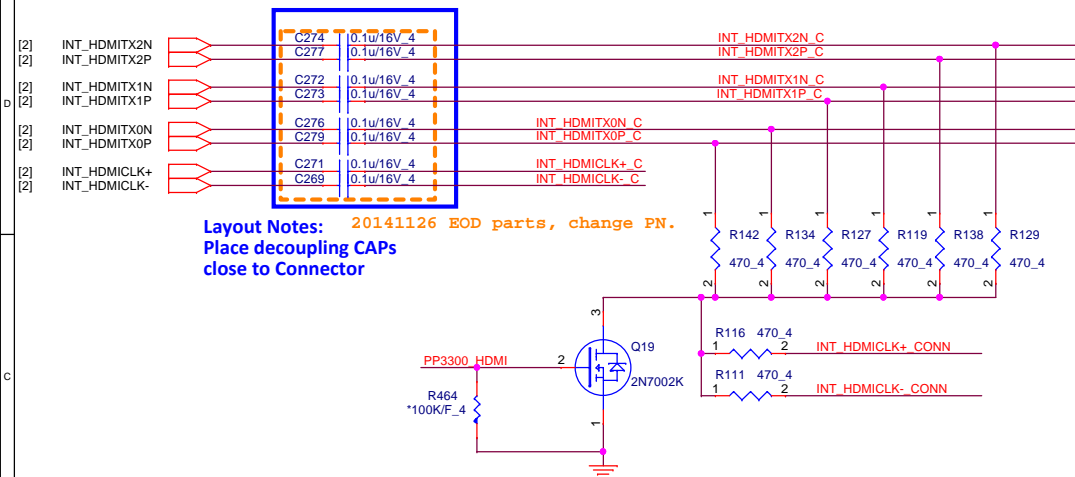


Quanta Computer Inc.

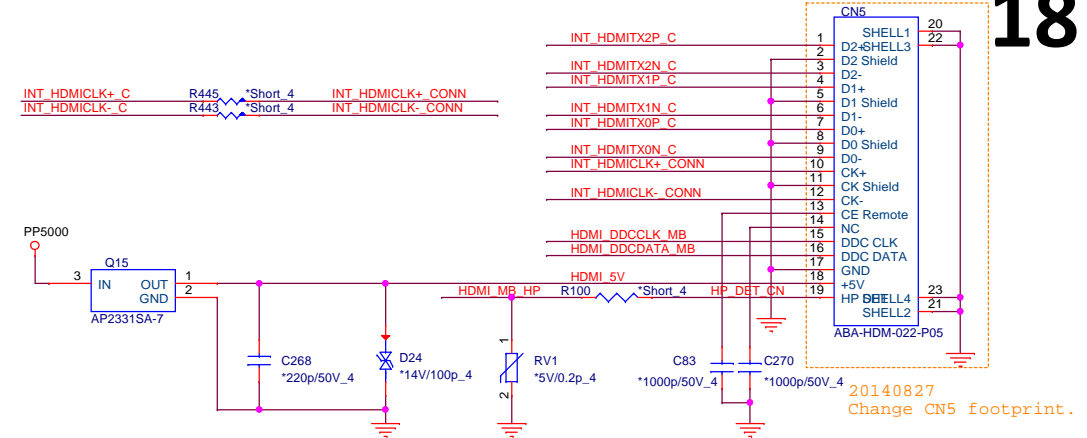
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Google Debug		
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HDMI Cost Reduced level shift (HDM)

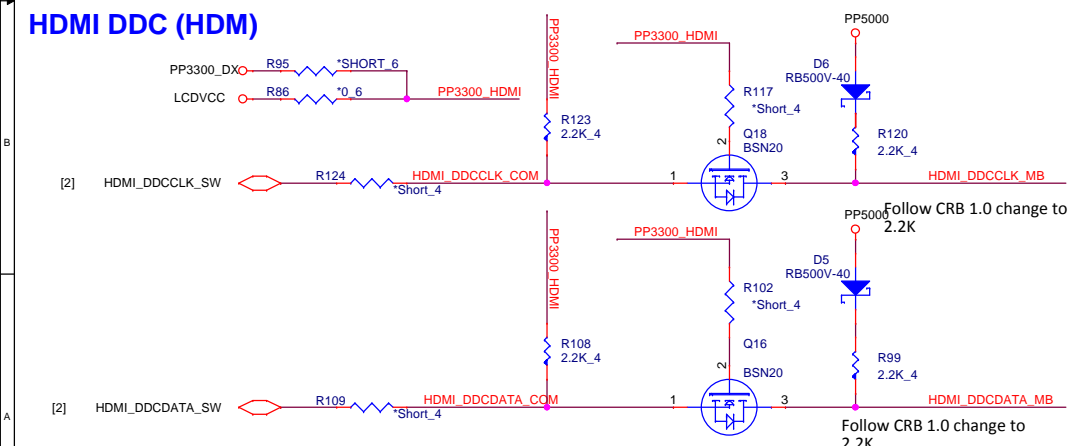


HDMI connector (HDM)

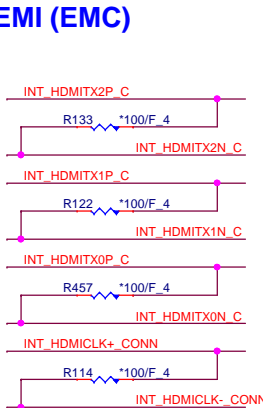


18

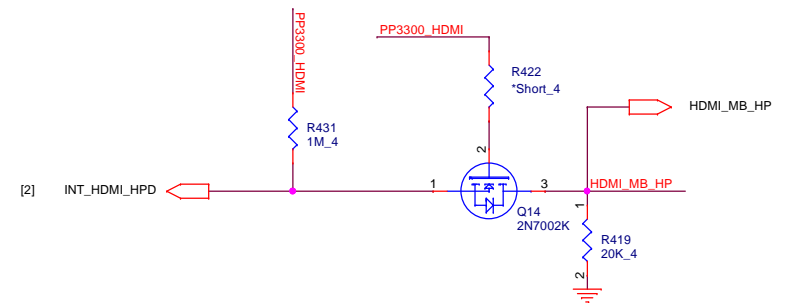
HDMI DDC (HDM)



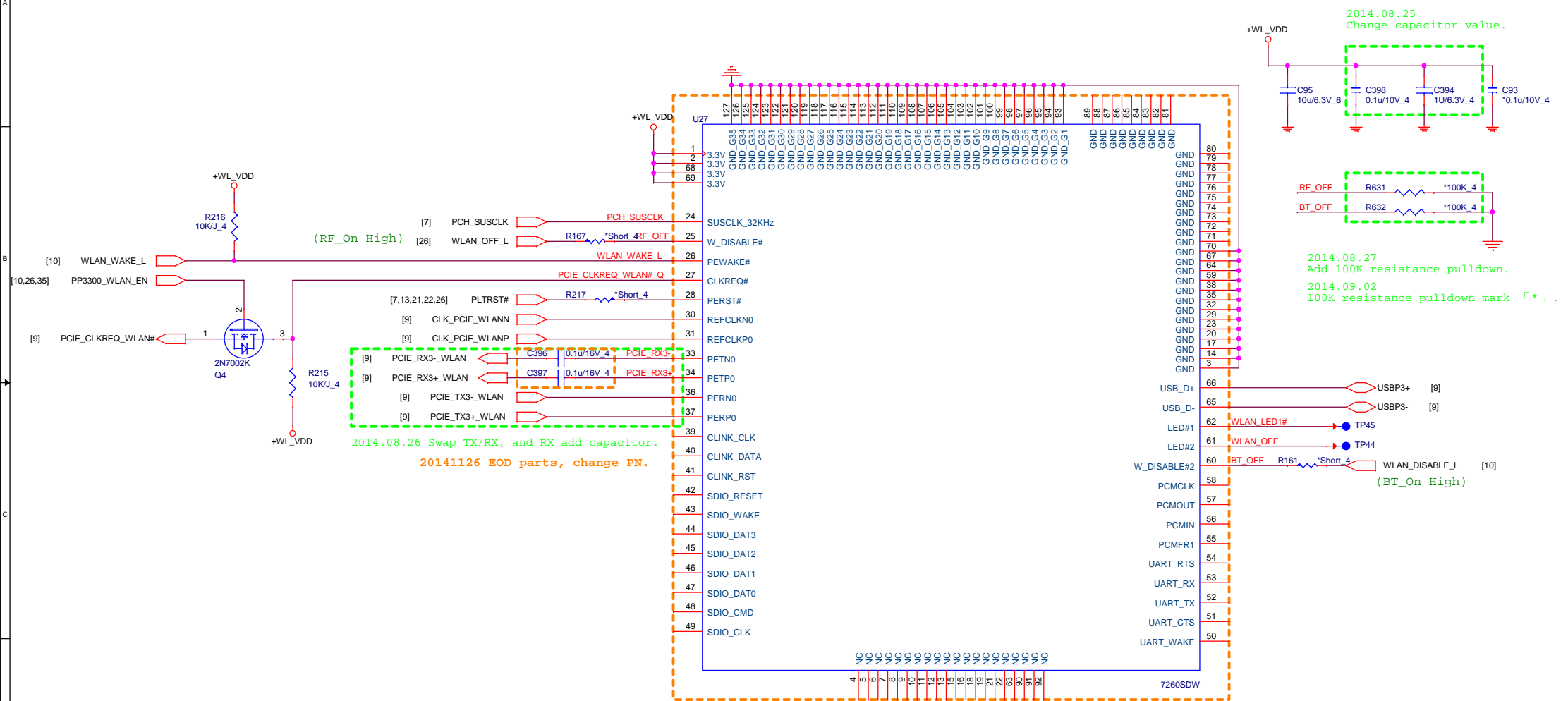
EMI (EMC)



HDMI-detect (HDM)



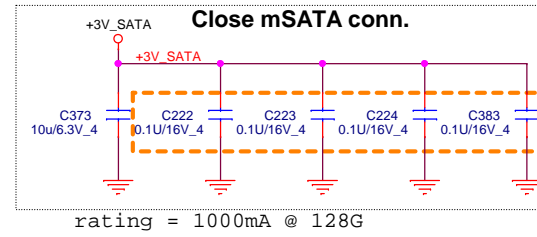
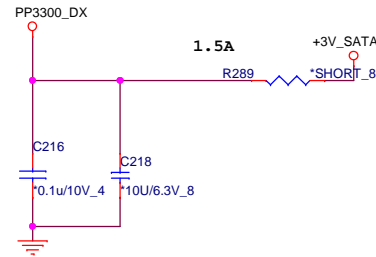
		Quanta Computer Inc. PROJECT : ZHNB	
		HDMI	Rev A
Size	Document Number	Date: Thursday, December 04, 2014	Sheet 18 of 39



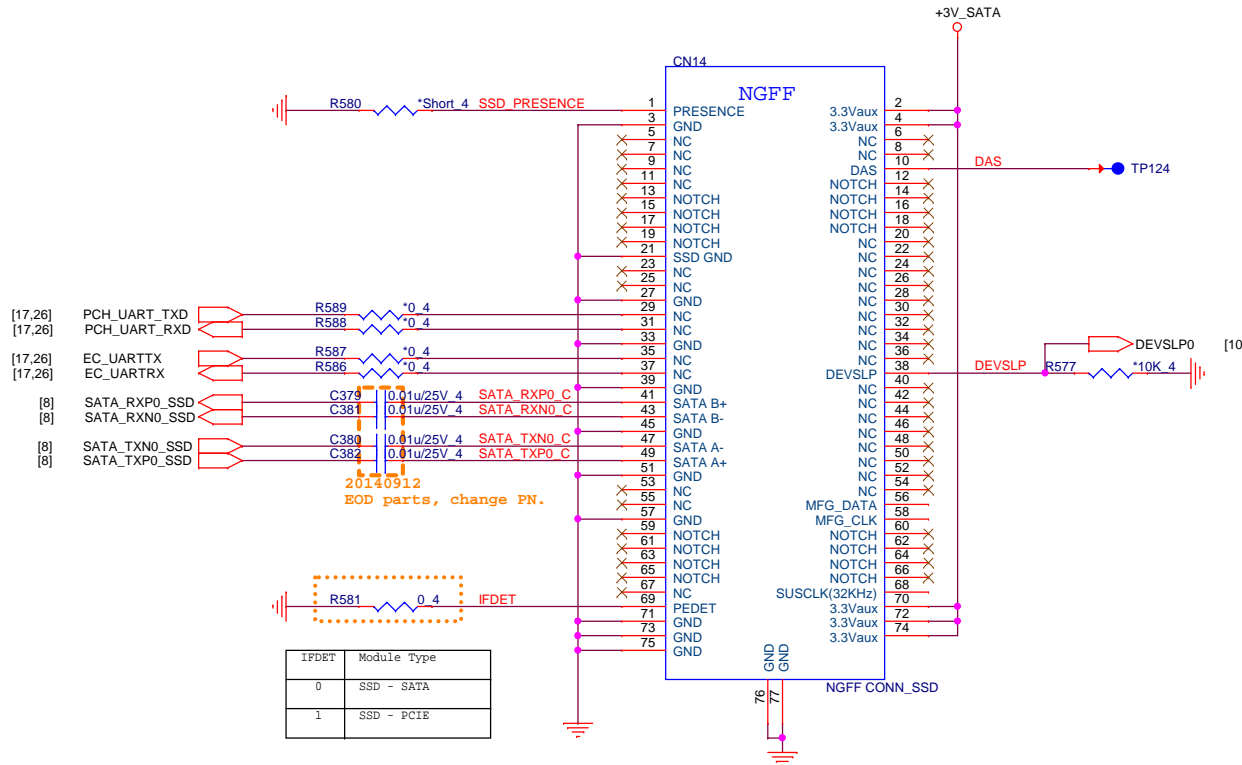
20140820 On board IC change to same as ZS8 connector
20140822 Return to another wifi onboard module 7260SDW
20140826 Change wifi onboard module 7260SDW footprint
20140909 Change wifi onboard module 7260SDW footprint
20141014 Change wifi onboard module 7260SDW PN.

NGFF SSD connector. San Disk SSD Card.

20



20141126 EOD parts, change PN.

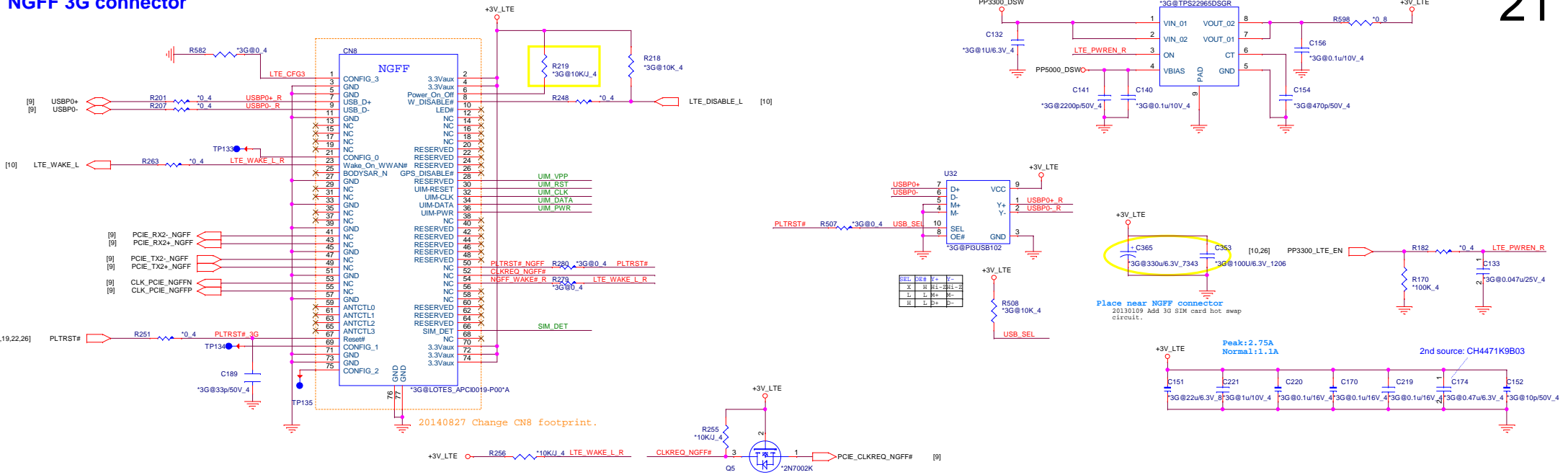


Quanta Computer Inc.
PROJECT : ZHNB

Size	Document Number	Rev
	NGFF SSD	A

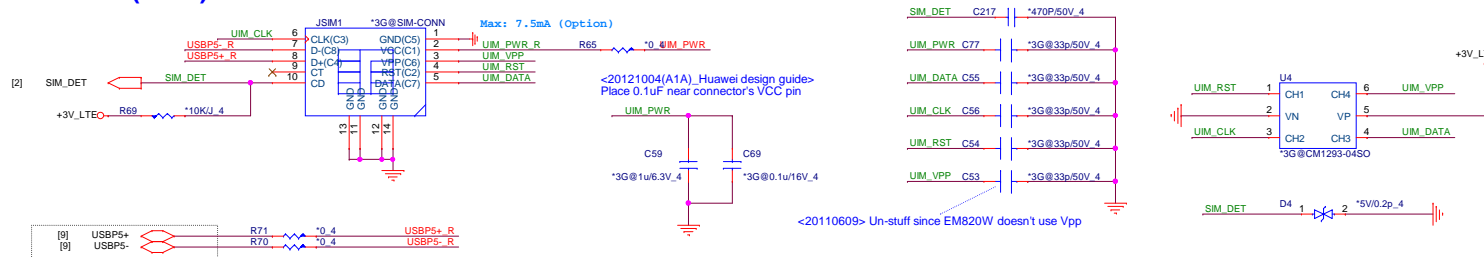
Date: Thursday, December 04, 2014 Sheet 20 of 39

NGFF 3G connector



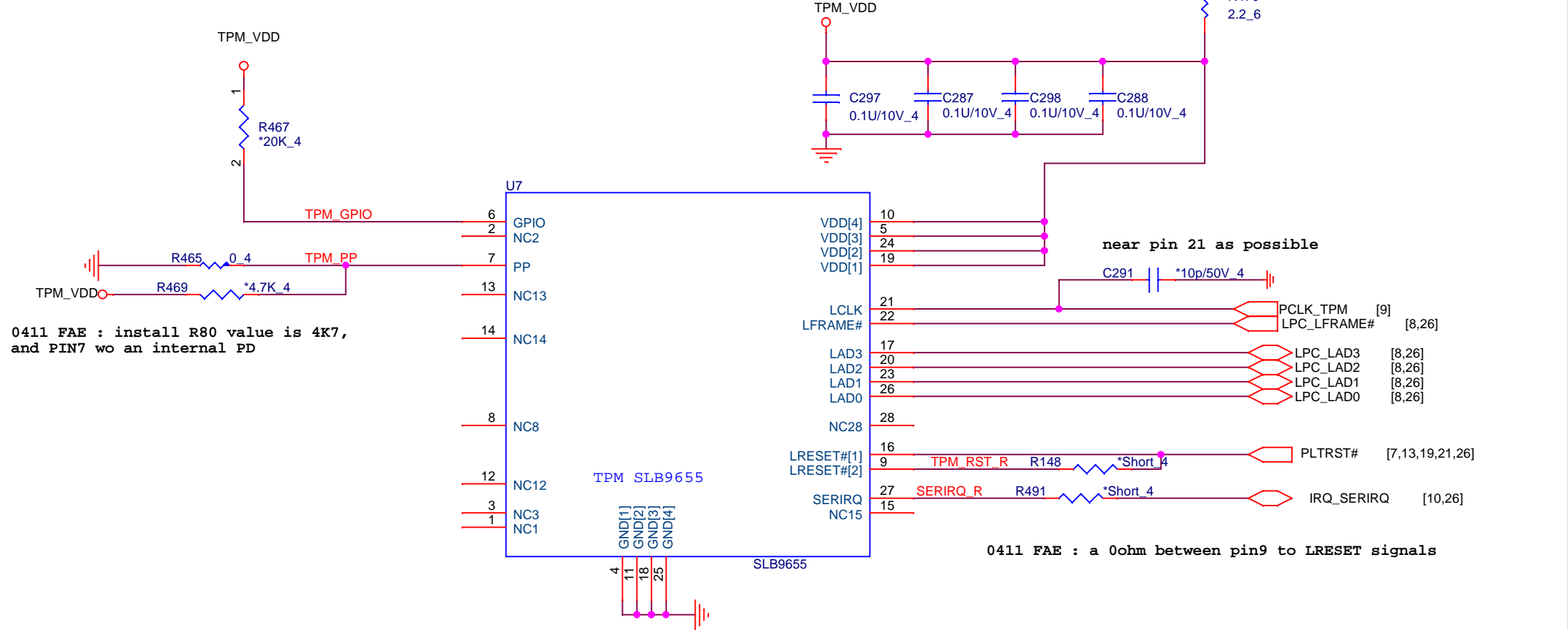
MultiMedia SIM (MNC)


<Layout Notes> Keep USIM signals max length within 8000mils.



TPM (TPM)

22

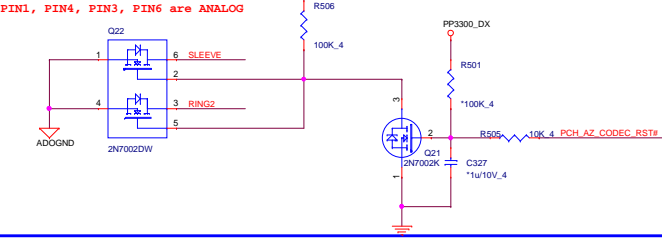
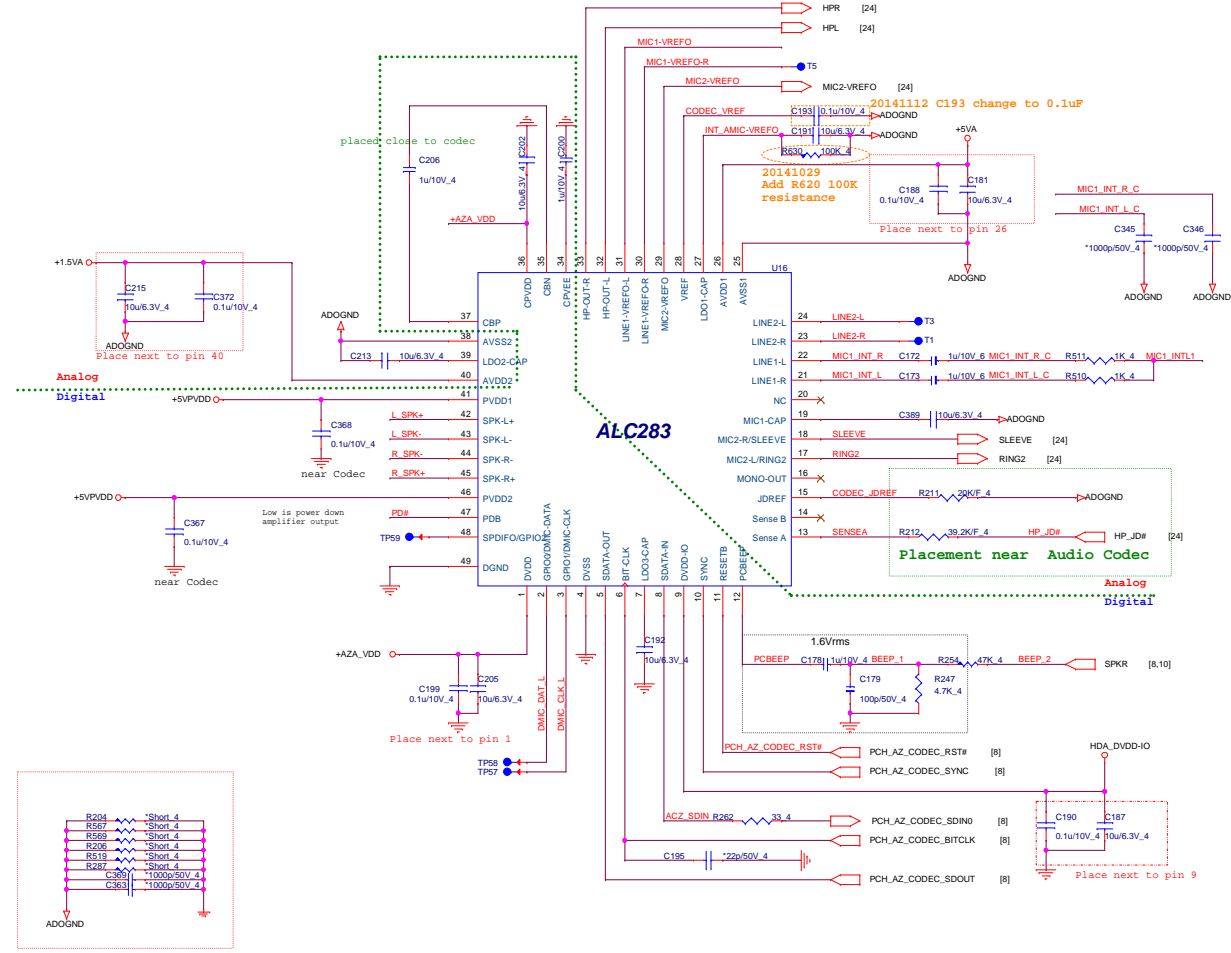




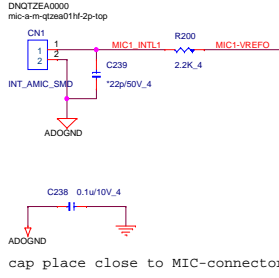
Quanta Computer Inc.

PROJECT : ZHNB

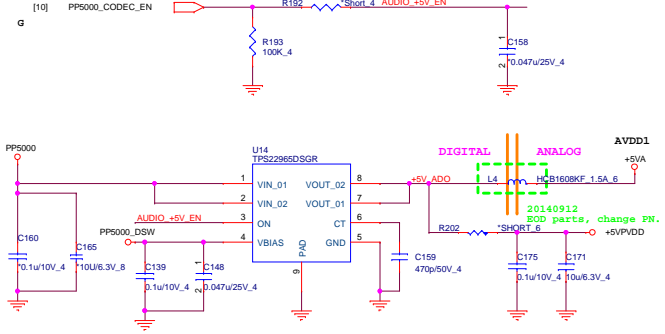
Size	Document Number	Rev A
TPM SLB9655 / LED		
Date:	Thursday, December 04, 2014	Sheet 22 of 39



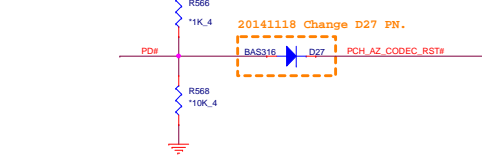
INT MIC array



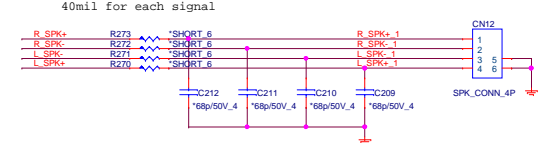
Codec PWR 5V(ADO)



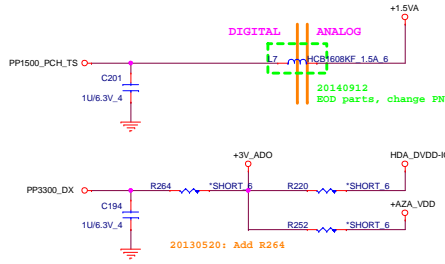
Mute(ADO)



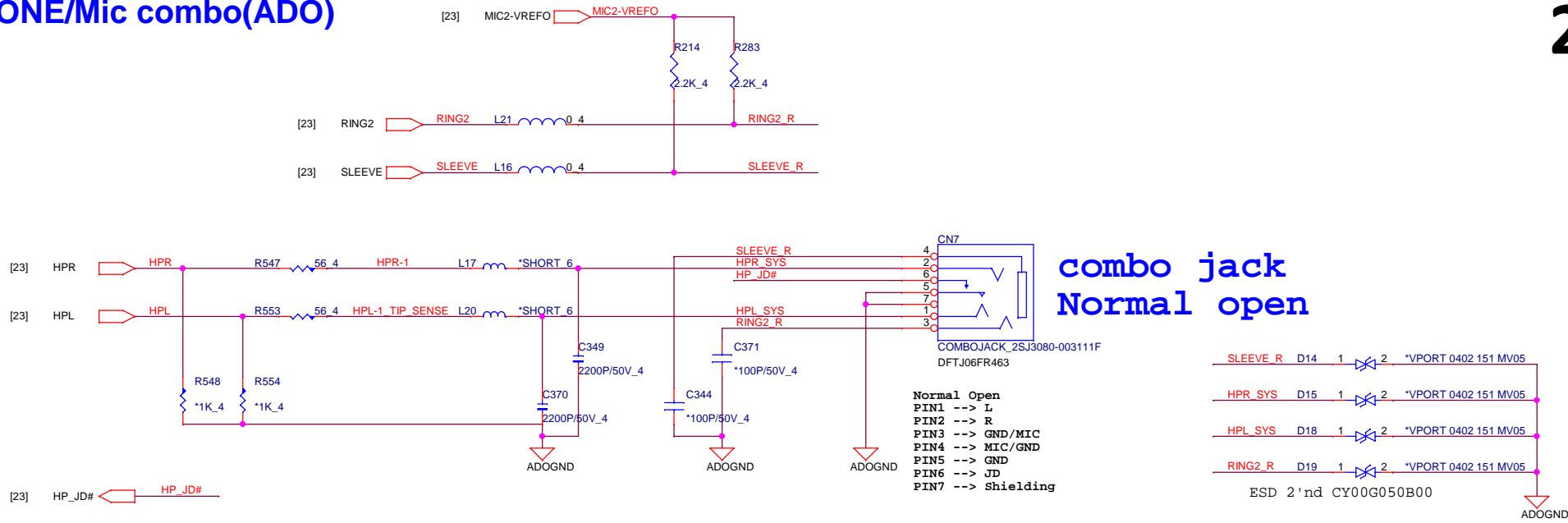
Internal Speaker

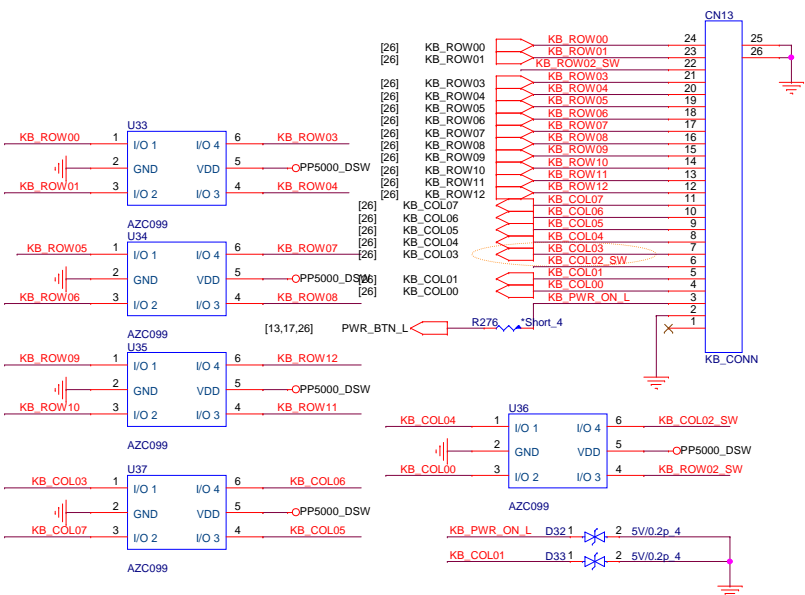


Codec PWR 3V/1.5V(ADO)

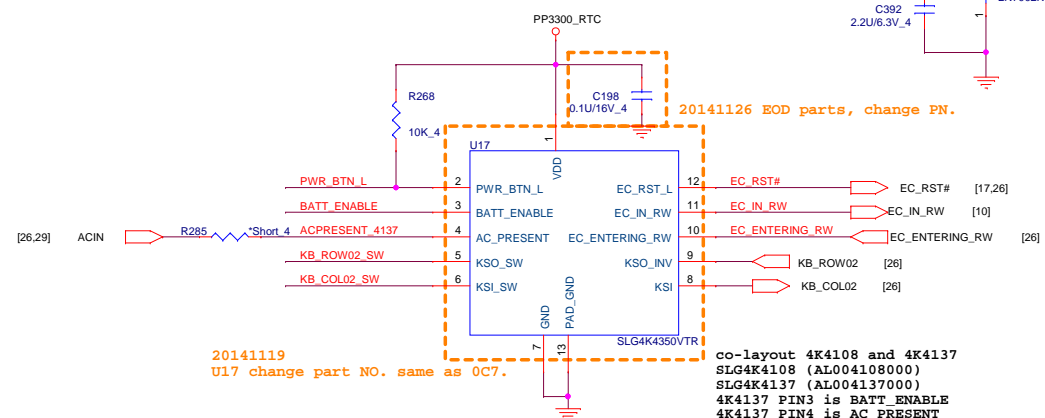
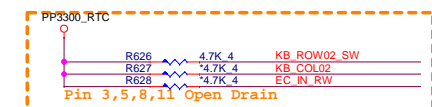


HEADPHONE/Mic combo(ADO)





HOLELESS RESET 2-CHIP(KBC)

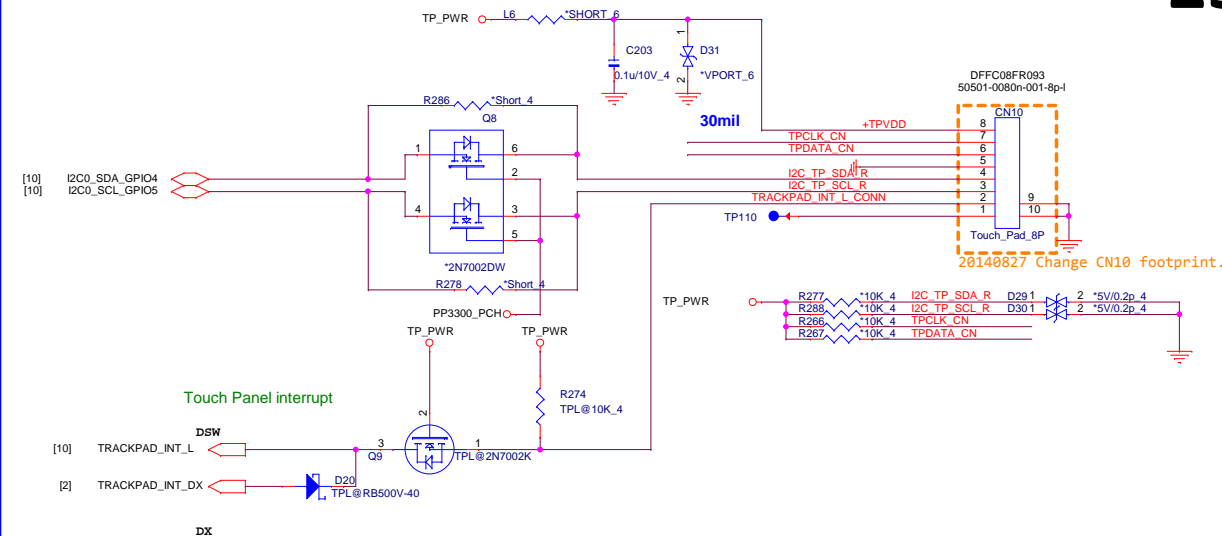


Connect to EC reset pin

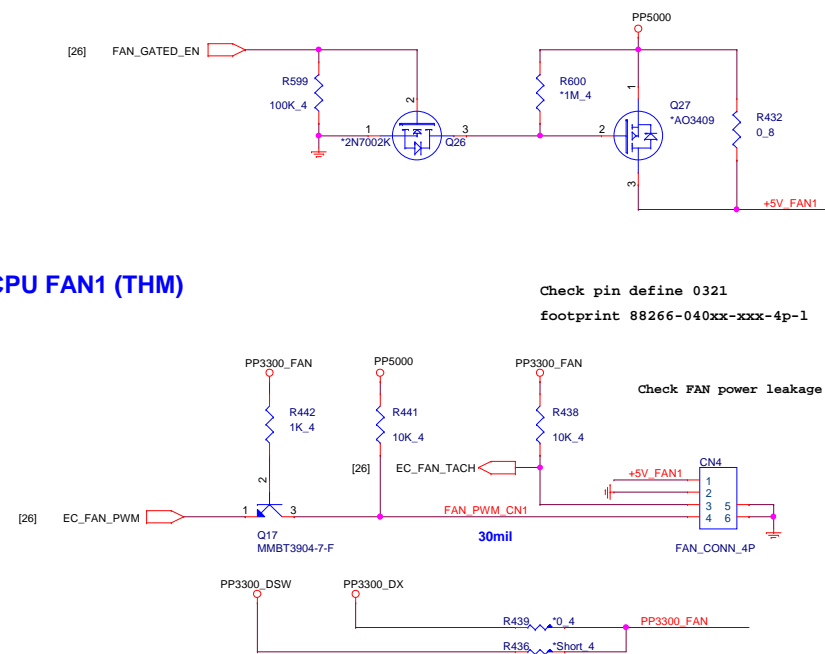
Connect to GPIO on CPU
with PU to GPIO power
well

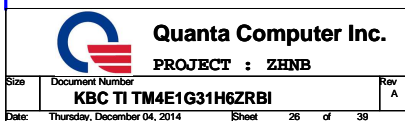
Connect to EC pin C5 (must
be low when EC IN RESET)

TOUCHPAD BOARD CONN (TPD)



CPU FAN1 (THM)







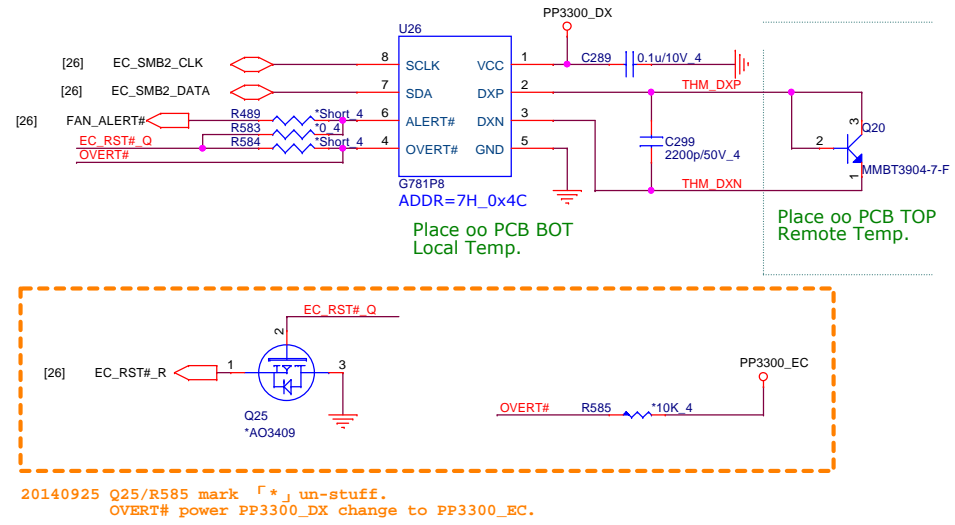
[17,26]

HOLE15
*H-C91D91NP

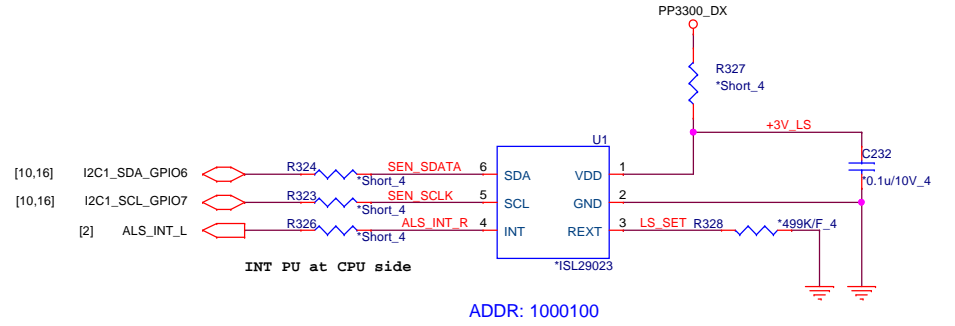
[8.26]

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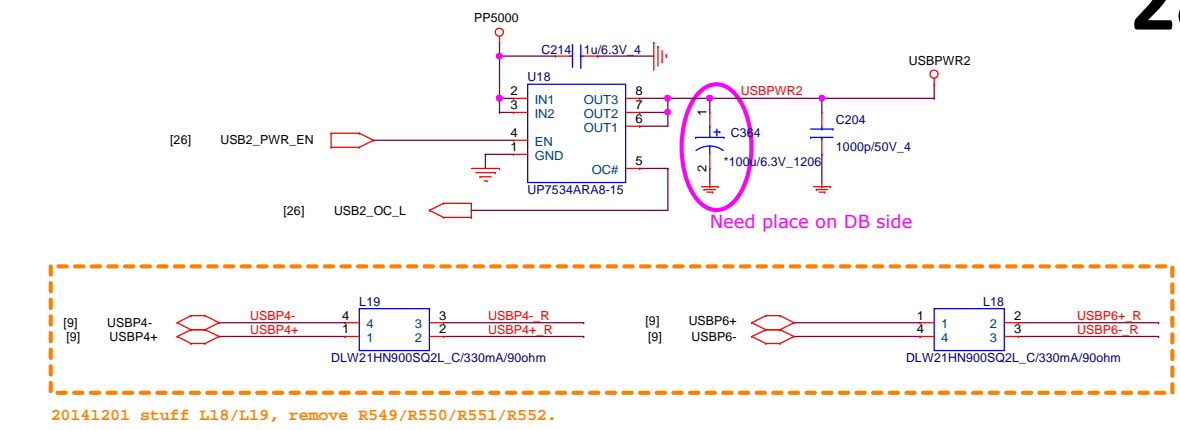
Thermal Sensor(THM)



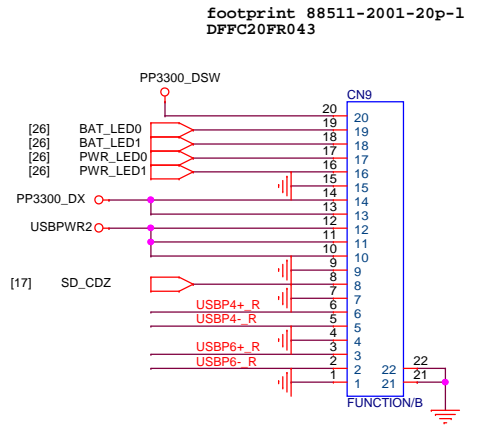
Light sensor & TP (SER)



FUNCTION DB



HSR	+3VPCU
	LID_OPEN_L
	GND
LED	+3VPCU
	LED x 4
	GND
USB	+3V x 2
	GND x 2
	USBP0+
	USBP0-
	GND x 2
CR	CR_DET
	+3V x 2
	USBP6+
	USBP6-



Quanta Computer Inc.
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Size	Document Number	Rev
	DB/ALS/Thermal sensor	A
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TDC : 0.75A
PEAK : 1A
Width : 40mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

+DDR_VTT_RUN

Greater than or equal 40mil

20141201
Capacitor 4.7uF Change to 10uF.

1.35 Volt +/- 5%
TDC : 3.35A
PEAK : 4.46A
OCP : 6A
Width : 140mil

Close to output cap

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (main on off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=6A
L ripple current
= $(19-1.35)*1.35/(3.3u*400k*19)$
=0.95A
Vtrip=[$6-(0.95/2)$]*14mohm
=0.07735V
Rlimit= $0.07335/10uA*8=61.88Kohm$

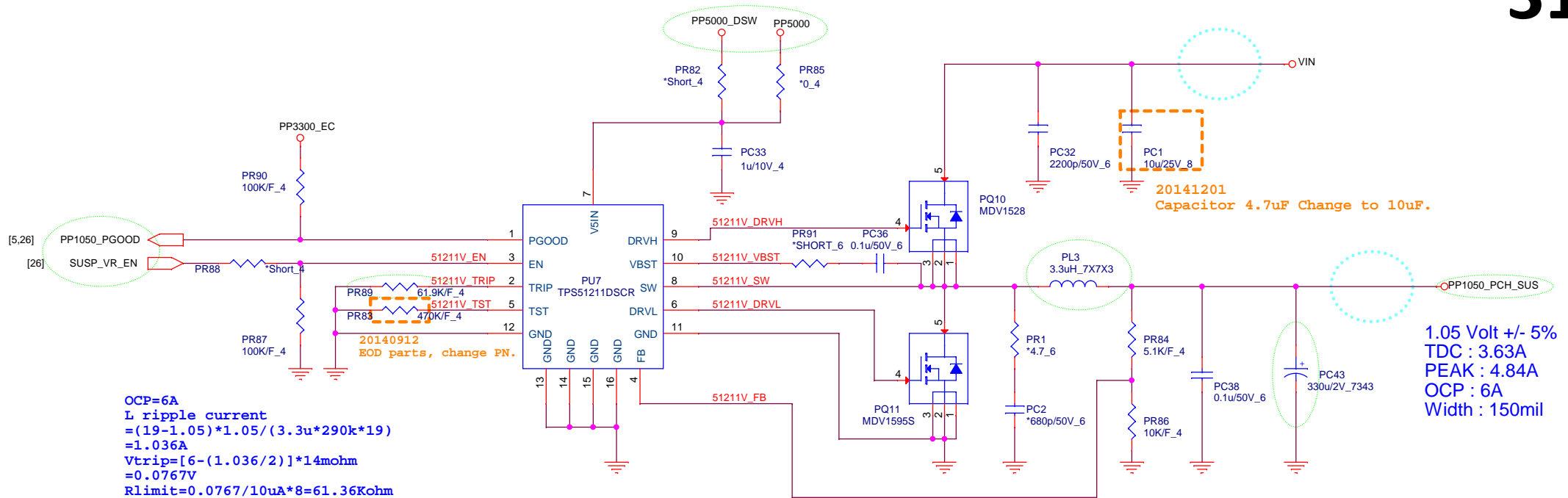


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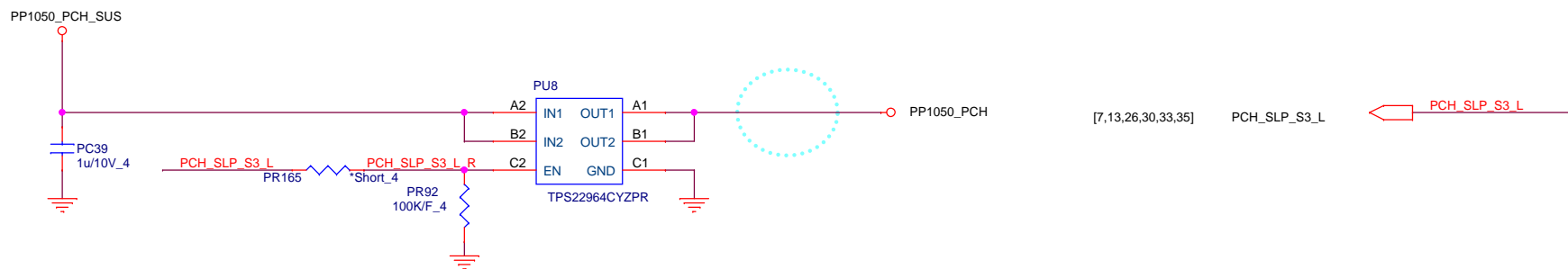
PROJECT : ZHNB

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	A

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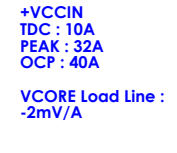
place at PQ37 area

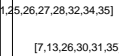


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PROJECT : ZHNB

Size Document Number
+1.05V(TPS51211) Rev A

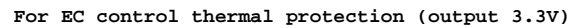
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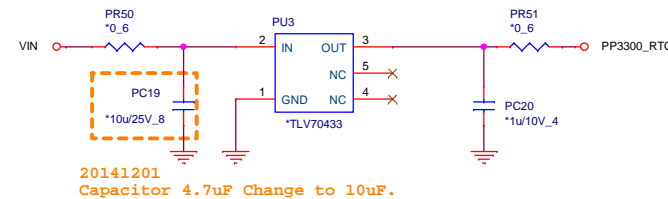








[26,34]



PP5000_EN

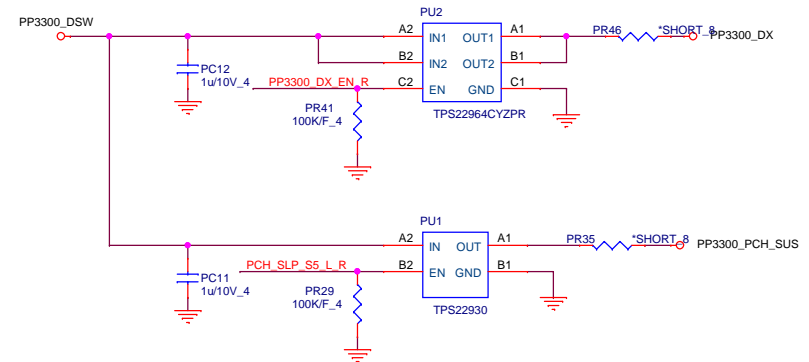
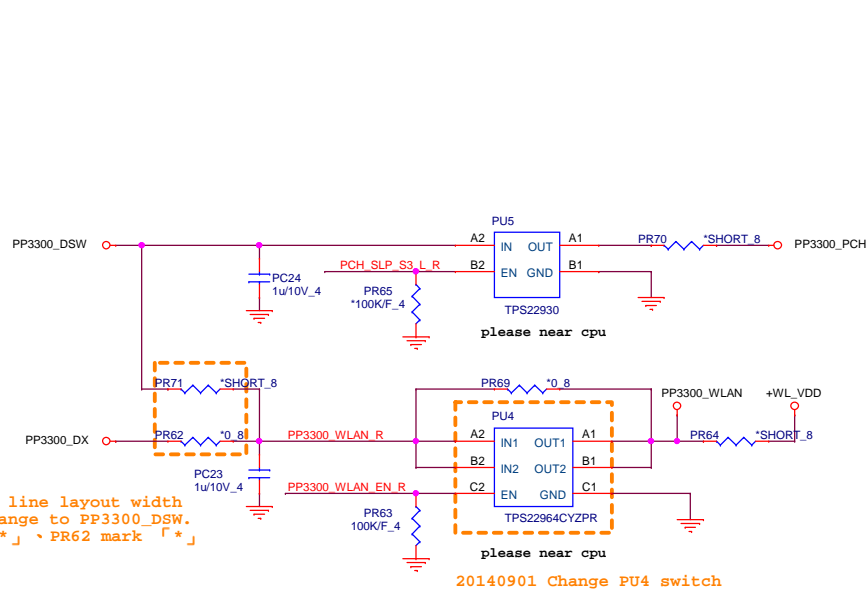






[7,13,26,30,31,33] PCH_SLP_S3_L  PCH_SLP_S3_L PR166  *Short_4 PCH_SLP_S3_L_R



[26] PP3300_DX_EN  PP3300_DX_EN PR167  *Short_4 PP3300_DX_EN_R

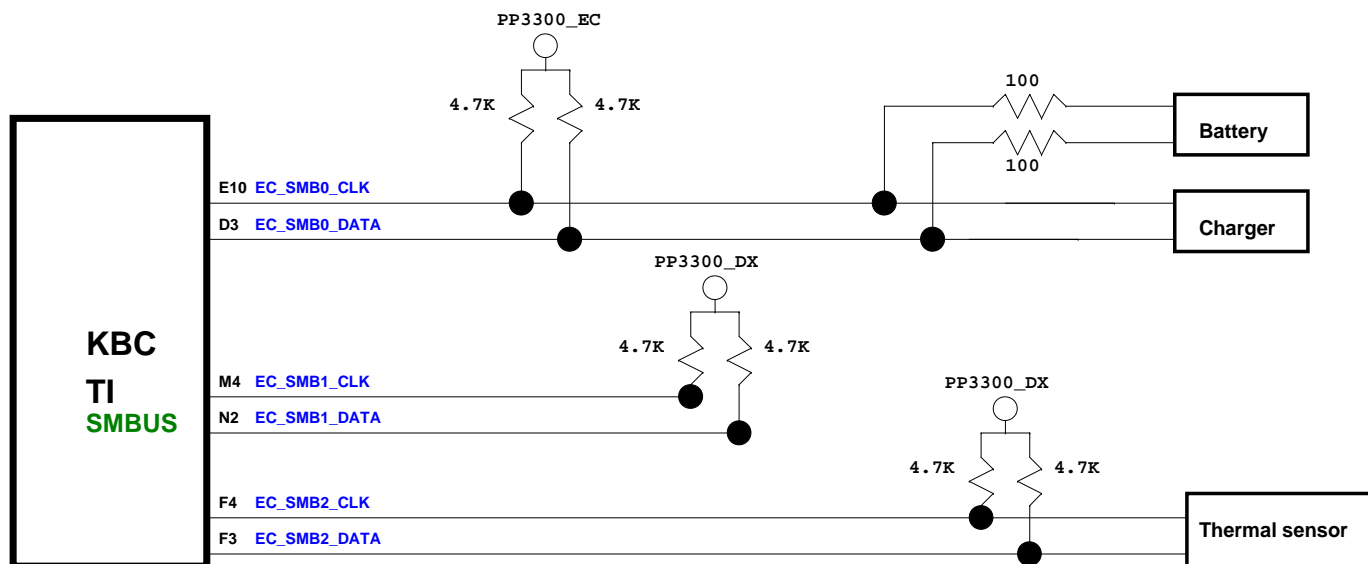
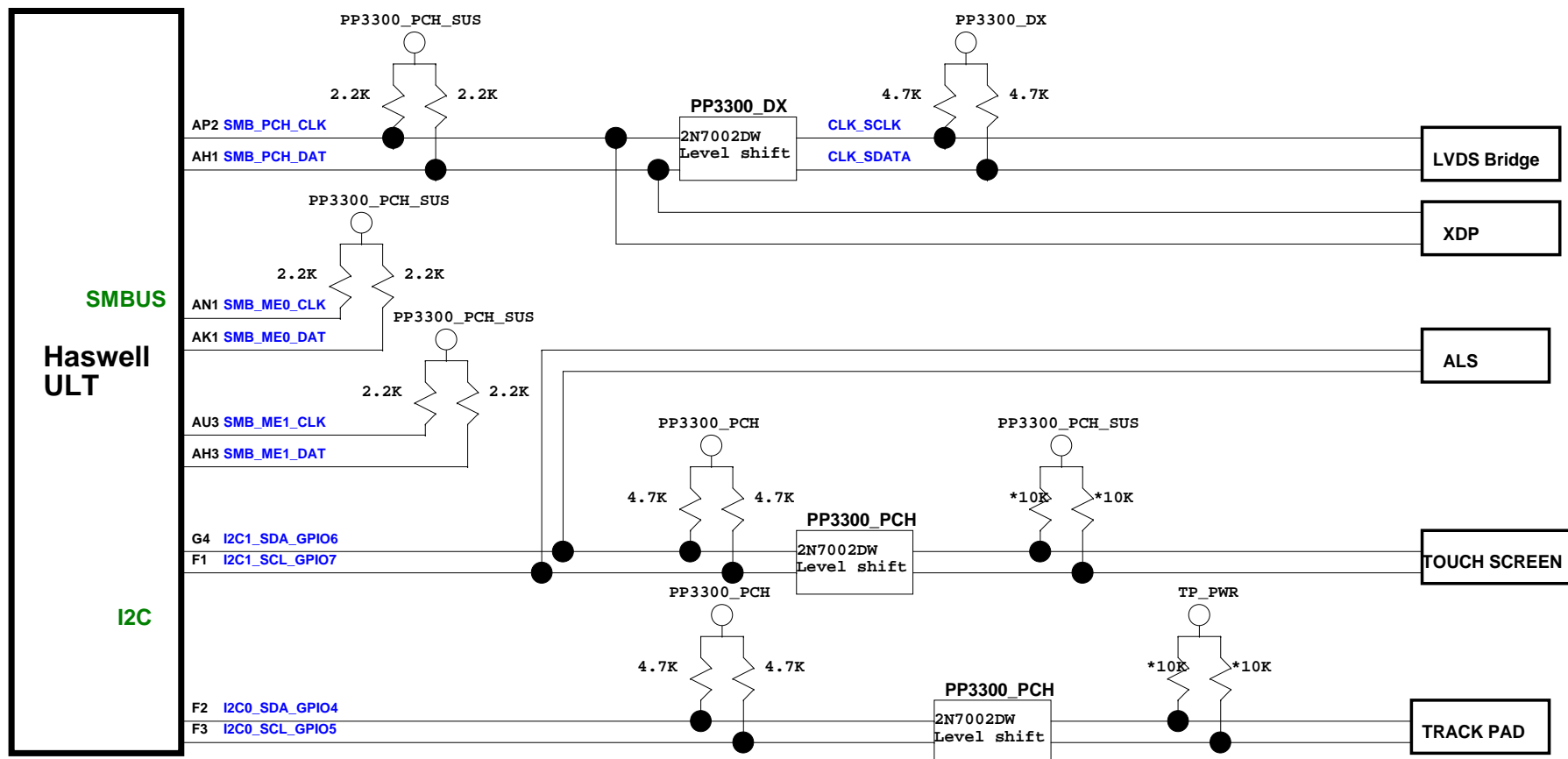
[10,19,26] PP3300_WLAN_EN  PP3300_WLAN_EN PR168  *Short_4 PP3300_WLAN_EN_R



4/24 modify

[7,26] PCH_SLP_SUS_L  R115  *Short_4 PCH_SLP_S5_L_R

[7,13,26,30] PCH_SLP_S5_L  PCH_SLP_S5_L R112  *0.4



Model	Version	CHANGE LIST	
ZHNB	1A-1	201408/21 Page16: LCD conn. I2C1, SDA, GPION, gpio reserve a 15uF capacitor. 201408/21 Page16: Touch panel level shift Q13 FET change to FT113BK. 201408/22 Page19: Wifi U27 change to another onboard module 7268SDW. 201408/22 Page21: NCP137 / S23 mark r_{s2} .	
	1A-2	201408/27 Page19: Change wifi onboard module 7268SDW footprint. 201408/27 Page19: Pin W, DRABLE2 / W, DRABLE2 add 100K resistance pull-down. 201408/27 Page18: Change L435 conn. CN3 footprint. 201408/27 Page18: Change RDH1 conn. CN5 footprint. 201408/27 Page21: Change NCP137 / S23 conn. CN8 footprint. 201408/27 Page25: Change touchpad board conn. CN10 footprint. 201408/27 Page25: Change VCCDE P79 footprint.	
	1A-3	201409/1 Page14: Change LDO PC14 switch.	
	1A-4	201409/2 Page15: LDO PR71 cancel r_{s2} + PR82 mark r_{s2} . 201409/2 Page19: Wifi 100K resistance B631/B632 mark r_{s2} .	
	1A-5	201409/9 Page26: Implant P873 for battery enable. 201409/9 Page19: Change wifi onboard module 7268SDW footprint.	
	1A-6	201409/12 Page16: C16 EIO, change PN. 201409/12 Page21: C70VC300V350V2K3 EIO, change PN. 201409/12 Page23: L41,7 EIO, change PN. 201409/12 Page26: C20K322300V1,5 EIO, change PN. 201409/12 Page29: PCX7PJ1 EIO, change PN. 201409/12 Page36: PC100 EIO, change PN. 201409/12 Page11: PR8 EIO, change PN. 201409/12 Page33: PR89 EIO, change PN.	
	1B-1	201409/24 Page26: USB1A U3 P1P2 add C19910A.	
	1B-2	201409/25 Page26: Thermal MONSET Q25Resistance R585 mark r_{s2} un-stuff. OVERT5 power PF3300, DX change to PF3300_EG.	
	1B-3	201410/14 Page19: Change wifi onboard module 7268SDW PN.	
	1B-4	201410/16 Page29: Change DC-to PN. (new module)	
	1B-5	201410/21 Page23: I2041 register enable TTP CN15 P0P51 add PF1059_PCH_SUS, P50 PF1059_PCH000 change to VCCST_P0BGD.	
	1C-1	201410/29 Page23: Code pin27 add 100K resistance. 201410/29 Page21: PC40 EIO, change PN.	
	1C-2	201411/07 Page26: Change U5 EC PN.	
	1C-3	201411/12 Page23: C193 change to R41uF. 201411/12 Page 46: 0 ohm resistance change to short pad.	
	1C-4	201411/18 Page23/Page26: change I227D28 PN.	
	1C-5	201411/19 Page25: U17 change part NO, name as BCT, add MONSET Q33. 201411/19 Page27: Remove R0E123 RATT_J201 pad, because enable control by U17. 201411/19 Page27: L41 SW change to un-stuff, because enable by U17. 201411/19 Page29: PR73 change to un-stuff, because enable control by U17.	
	1C-6	201411/20 Page26 Change EC, RRD, ID, ID2 change to High, ID3 change to Low, because EC change code.	
	1C-7	201411/25 Page16 Change TPS5R61Q13 to un-stuff, because no touch panel.	
	1C-8	201411/26 CB4103K1B03 EOS parts, change to CB4103K1B08	
	1D-1	201412/01 Page22 Change TPM power. 201412/01 Page24 Change EC use PN. 201412/01 Page27 Shift L124,L101,L19, remove R371/R372/R373/R374/R375/R376/R377/R378/R379/R380/R381/R382. 201412/01 Page29 Change DC-to footprint. 201412/01 PC13PC19PC311/PC8/P67/PC75 4.7uF change to 10uF.	